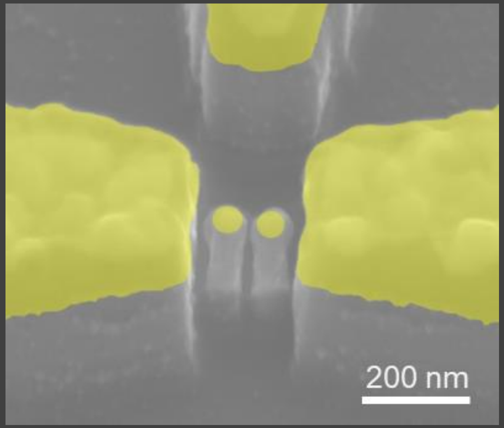
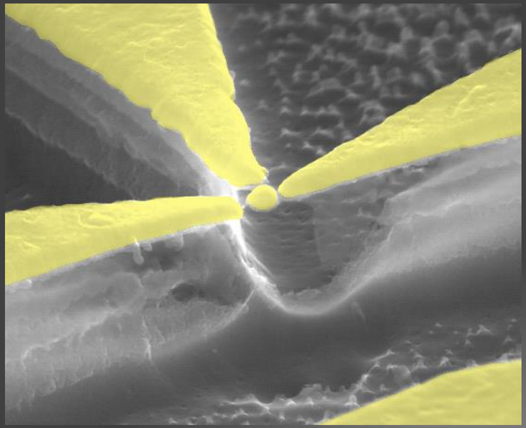
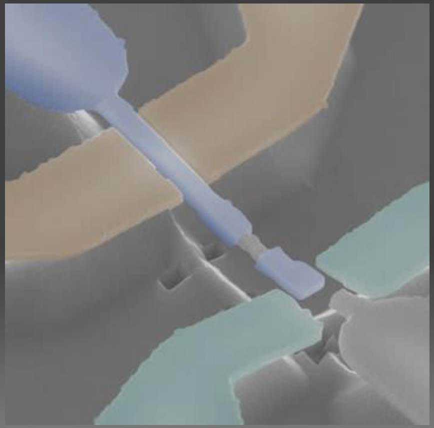
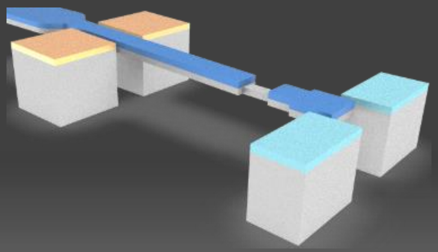
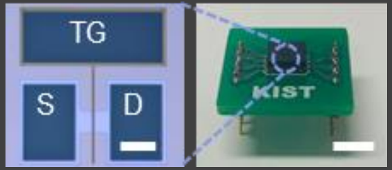
# Fabrication in Micro- and Nanoscale

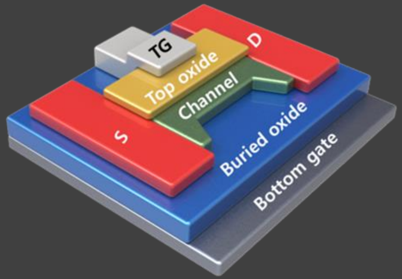


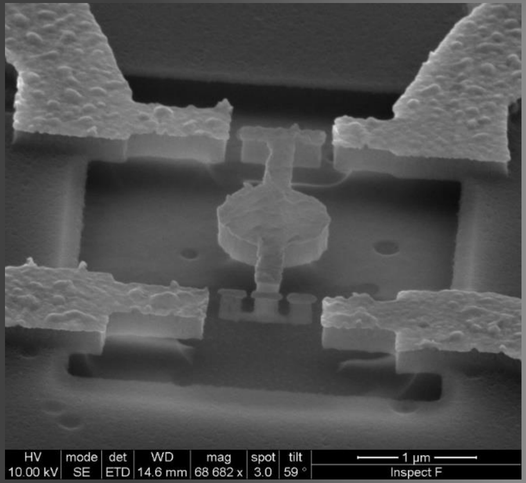


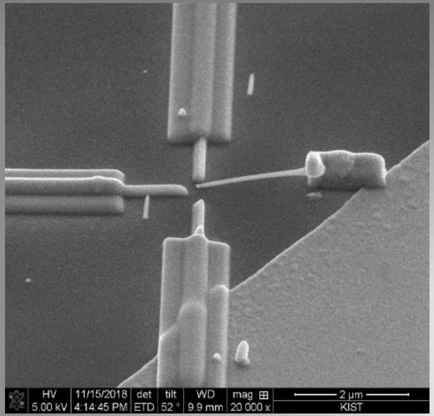


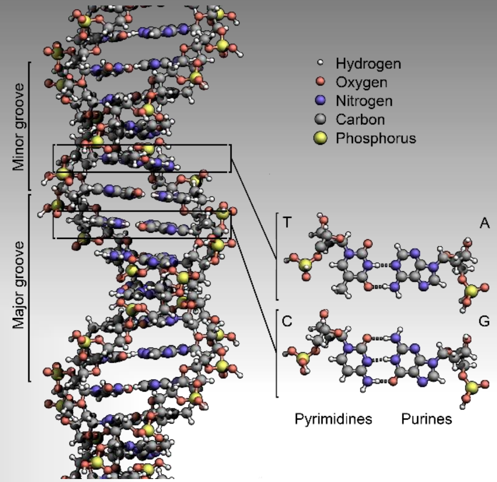












## KIST

## Chulki Kim

# AGENDA

- Top-down and bottom-up approach

# AGENDA

- Top-down and bottom-up approach
- Field Effect Transistor (FET) with dual gates
- Photolithography

  Reactive ion etching

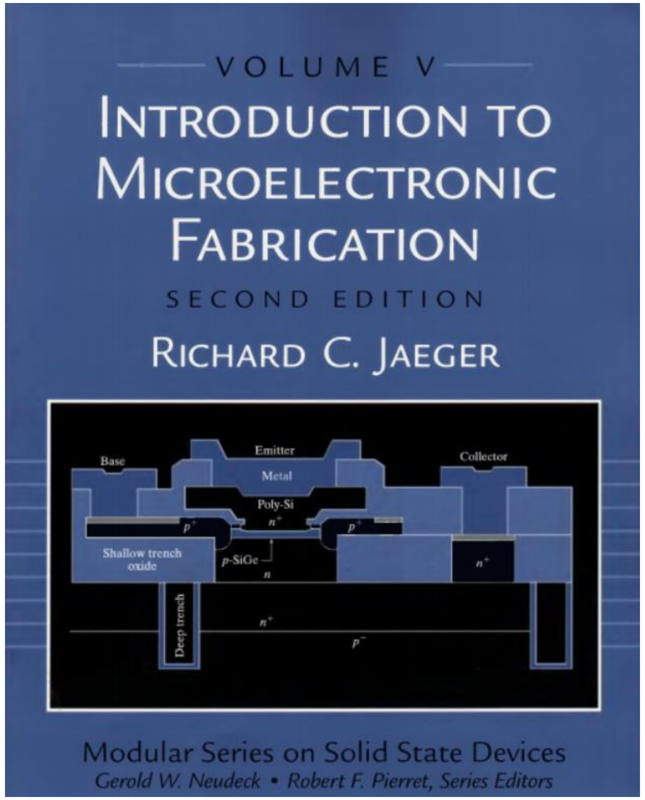
  Metal deposition

  Ion implantation

  Annealing

  Chemical vapor deposition

Microscale fabrication



VOLUME V

INTRODUCTION TO MICROELECTRONIC FABRICATION

SECOND EDITION

RICHARD C. JAEGER

Modular Series on Solid State Devices

*Gerold W. Neudeck • Robert F. Pierret, Series Editors*

# AGENDA

- Top-down and bottom-up approach
- Field Effect Transistor (FET) with dual gates
- Electron shuttles as Nanoelectromechanical systems (NEMS)

  Electron beam lithography

  Bosch Process

  Focused ion beam (FIB)

# AGENDA

- Top-down and bottom-up approach
- Field Effect Transistor (FET) with dual gates
- Electron shuttles as Nanoelectromechanical systems (NEMS)
- DNA-based nanostructure

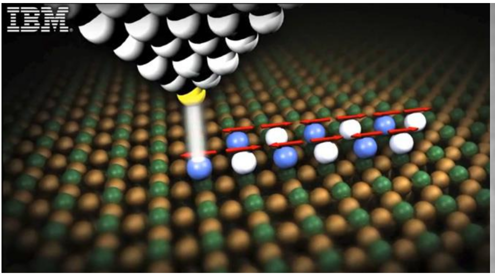
# AGENDA

- Top-down and bottom-up approach
- Field Effect Transistor (FET) with dual gates
- Electron shuttles as Nanoelectromechanical systems (NEMS)
- DNA-based nanostructure

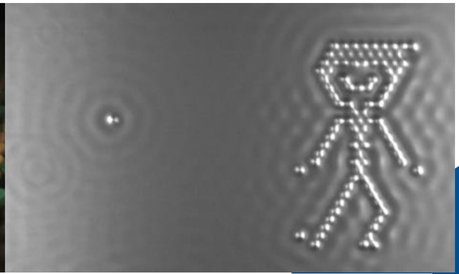
# Top-down and Bottom-up

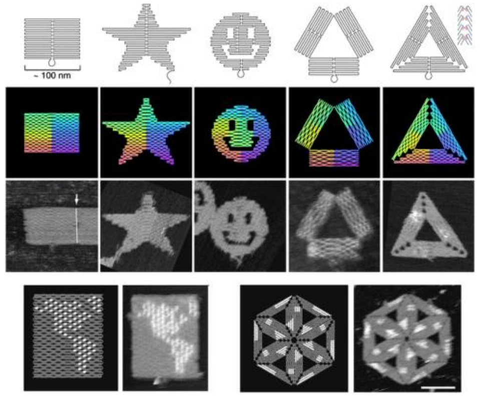
F. D. Natterer *et al.*,
*Nature* 543, 226 (2017).

Single-atom magnets (Ho/MgO)

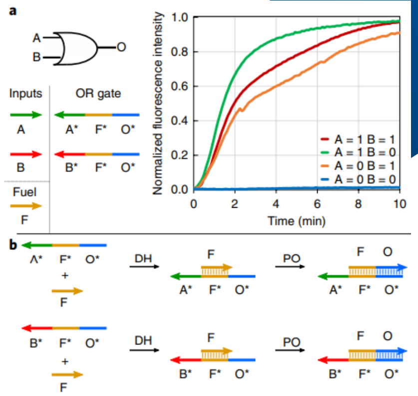


A Boy and His Atom:
The world's Smallest Movie
https://youtu.be/oSCX78-8-q0

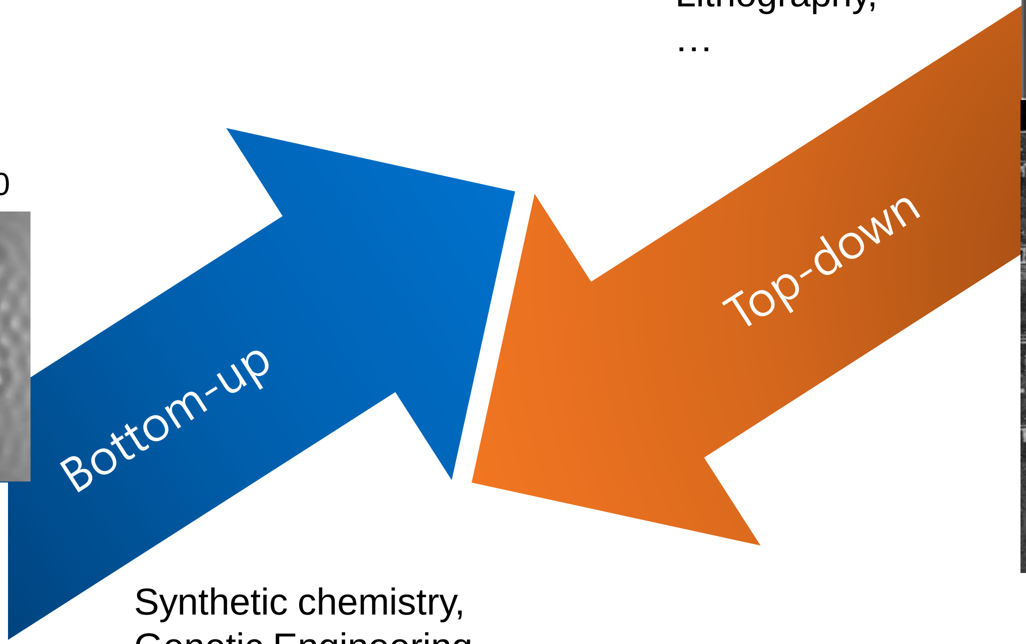




DNA
origami

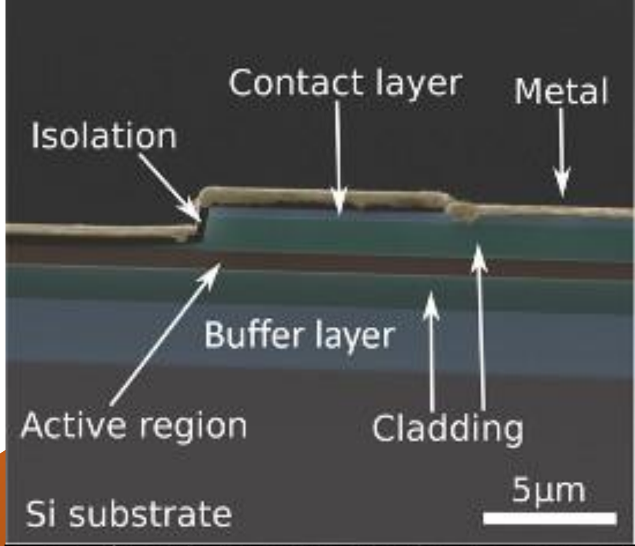


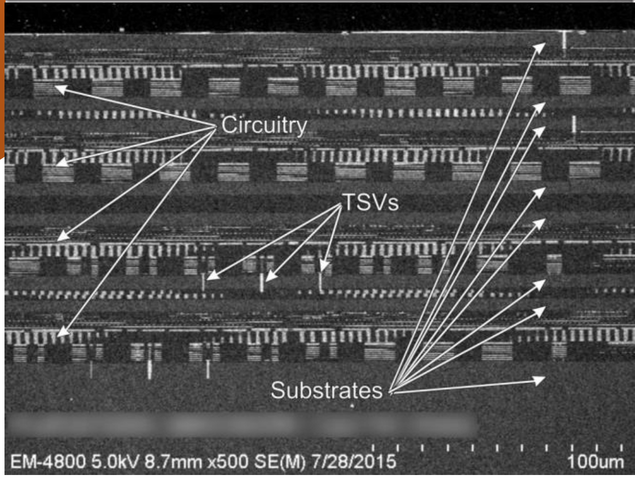
T. Song *et al.*,
*Nature* 14, 1075 (2019).



Lithography,
…

Synthetic chemistry,
Genetic Engineering,
Atomic manipulation,
…





Integrated circuit

# Bottom-up fabrication

- An additive process: atoms and molecules are used to build up the desired objects

- Advantages:

  The resolution is of atomic precision.

- Disadvantage:

  The limitation of large scale uniformity when up-scaling

# Top-down fabrication

- A subtractive process: material is removed to produce features of a controlled shape and size.

- Advantages:

  Enable to put the desired feature / entity in an exact location

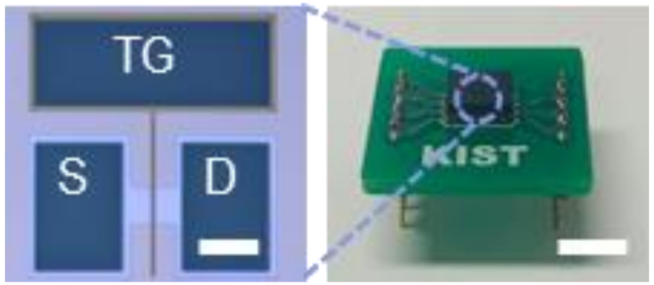
  Enable mass production

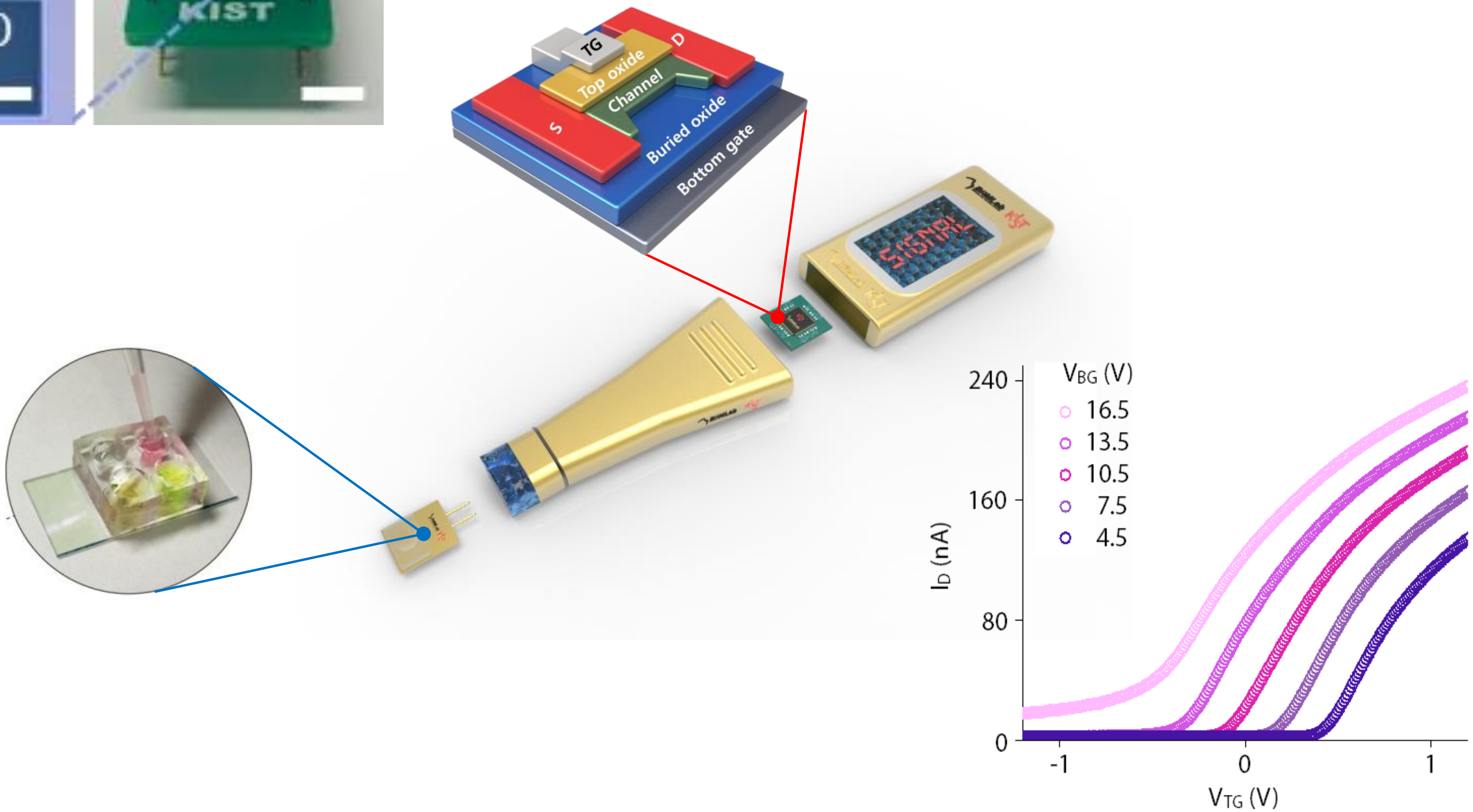
- Disadvantage:

  the resolution limitation due to the existing cutting tool technology (electron beam, ion beam, etc.)

# Field Effect Transistor (FET) with dual gates

# Motivation:
# On-site Avian Influenza (AI) virus detection





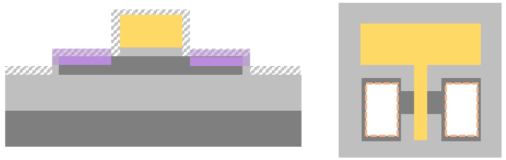
# FET Fabrication Flow

1. Active (Si channel) etching

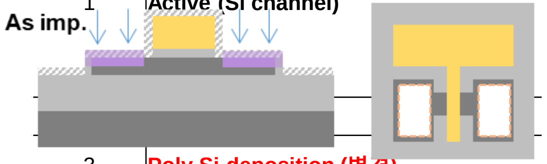
2. Gate dry oxidation

3. Electrode deposition

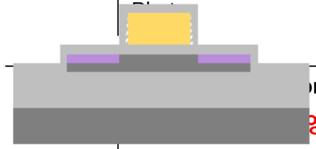
4. SiO2 cap ox.



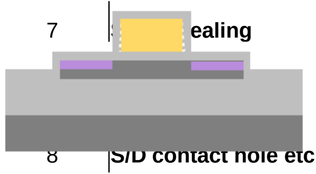
5. implantation



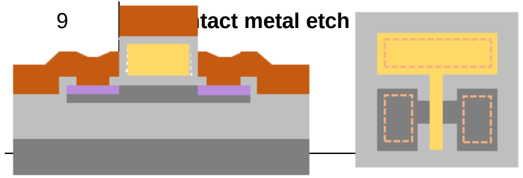
6. Annealing



7. Cap ox etch / passivation ox. dep



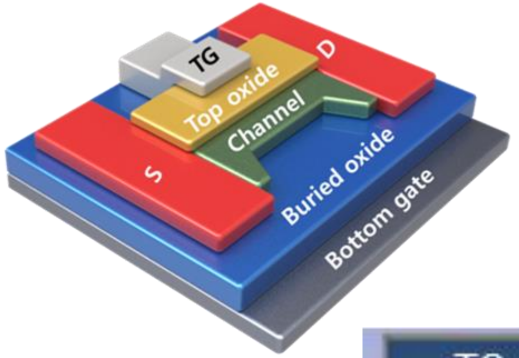
8. S/D contact hole etch / (Ti/TiN/Al/TiN) deposition

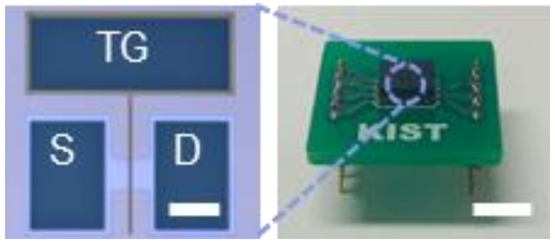


| No. | Process step |
|---|---|
| 1 | **Active (Si channel)** |
| 3 | Poly-Si deposition (변경) |
| 4 | **Gate etch** |
| | on |
| | 영역 close) |
| | Photo |
| | implant |
| 7 | ealing |
| 8 | **S/D contact hole etch** |
| | Photo. |
| | SiO2 cap RIE |
| | S/D (Ti/TiN/Al/TiN) deposition (변경) |
| 9 | **tact metal etch** |

9. S/D contact metal etch

10. $H_2$ anneal





# 1. Active channel formation

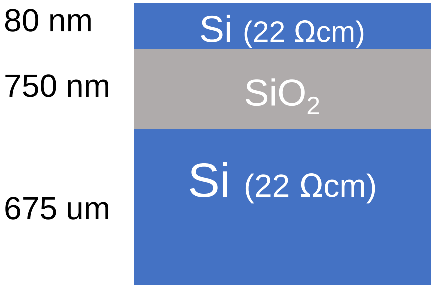
**1. Active (Si channel) etching**

- Wafer selection
- Photolithography
- Reactive ion etching (RIE)

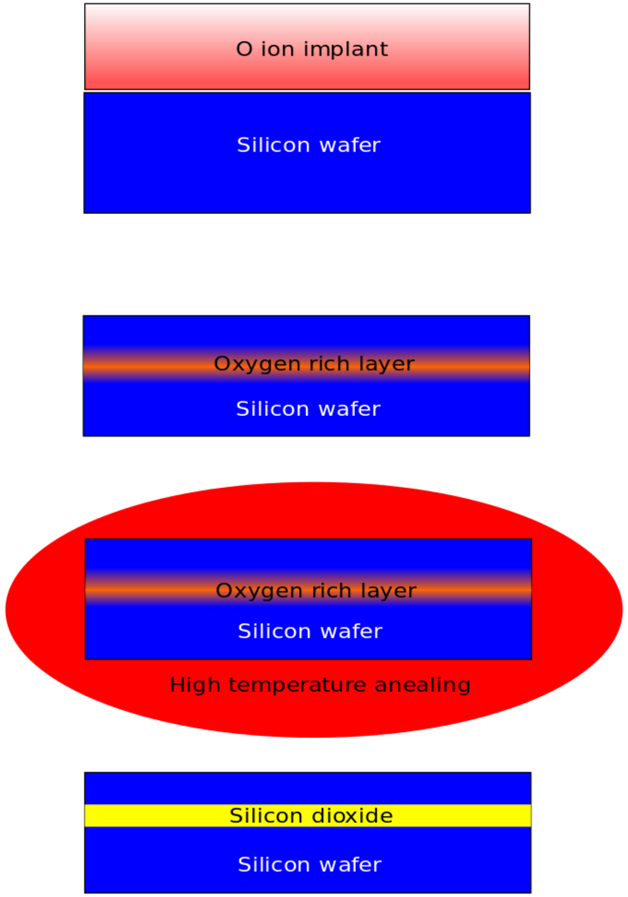
# Wafer selection

# Silicon on insulator (SOI) :

A layered silicon-insulator-silicon substrate
to reduce parasitic capacitance within the device

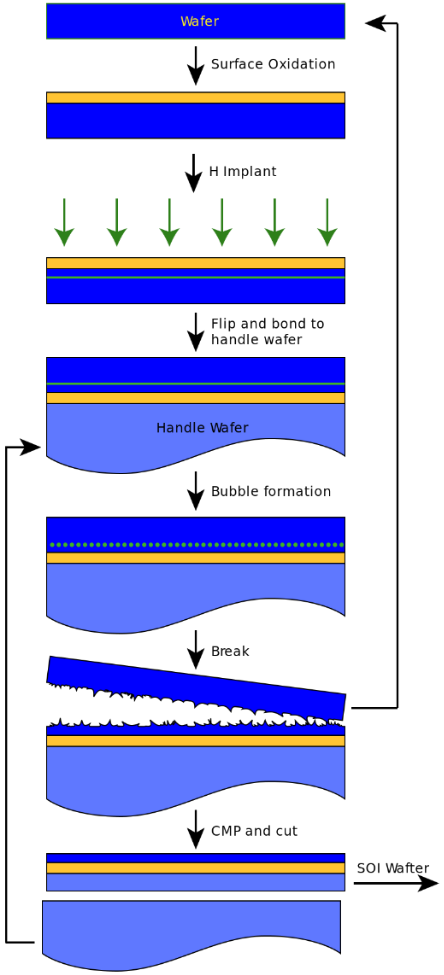


## SIMOX – Separation by Implantation of OXygen



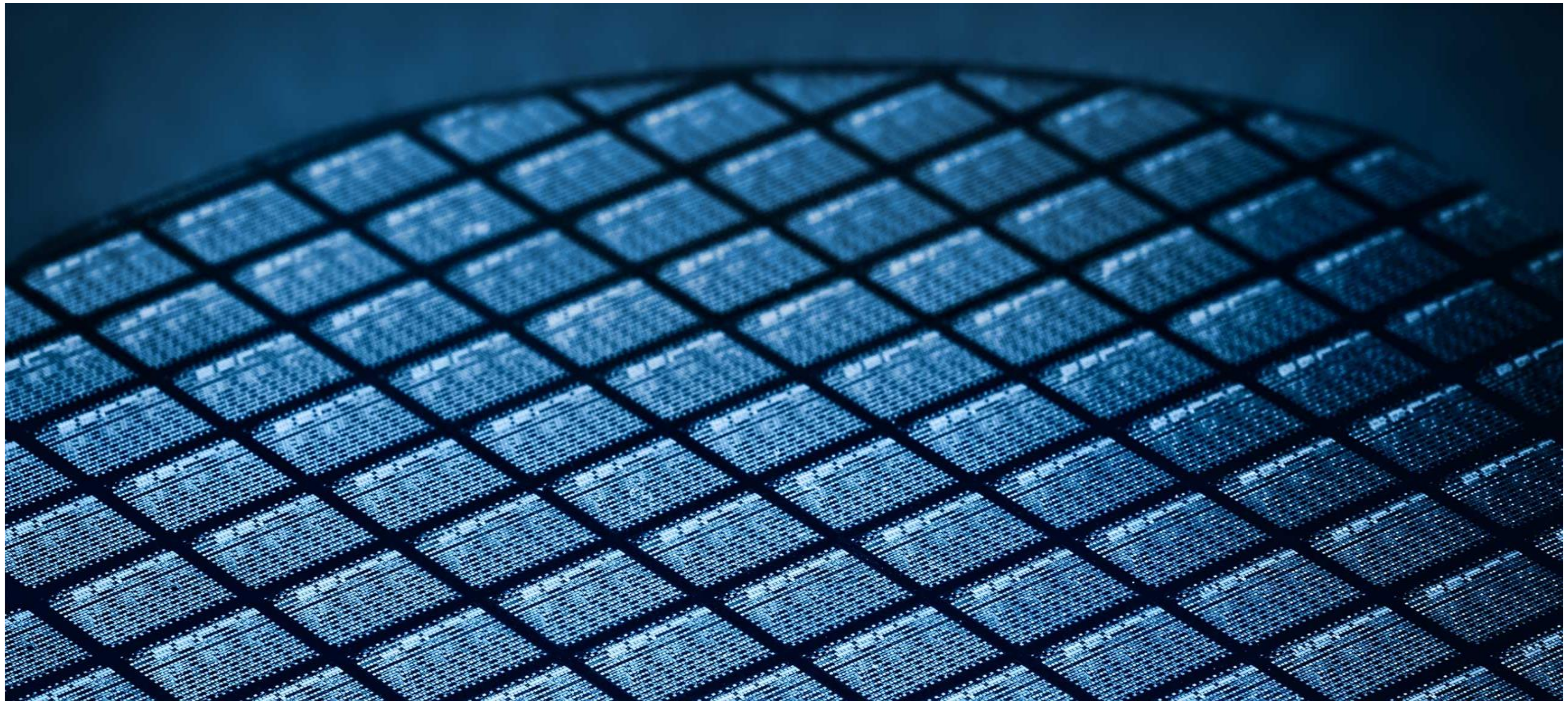
U.S. Patent 5,888,297 Issue data: Mar 30, 1999

## Wafer bonding – Smart Cut (Soitec)



U.S. Patent 5,374,564
Issue data: Dec 20, 1994

# Photolithography



- ✓ Photolithography uses light to transfer a geometric pattern from a photomask to a photosensitive chemical photoresist on the substrate. Photolithography is the standard method of printed circuit board (PCB) and microprocessor fabrication.

# Photolithography

- Clean wafers
- Coat with photoresist
- Soft bake
- Align masks
- Exposure pattern
- Develop photoresist
- Hard bake
- Etch a window

# Photolithography

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# Typical wafer cleaning processes

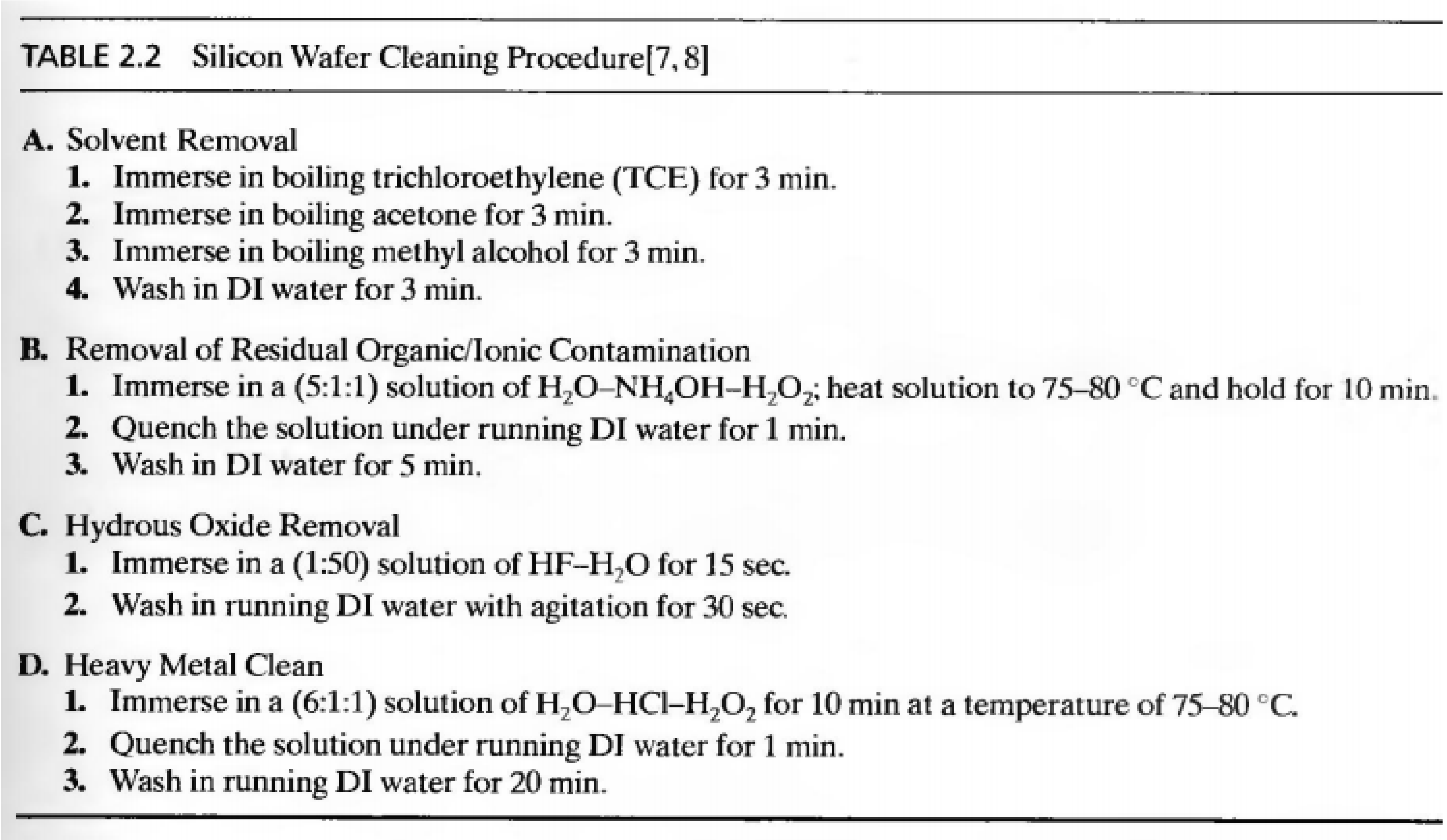


TABLE 2.2 Silicon Wafer Cleaning Procedure[7, 8]

**A.** Solvent Removal
  **1.** Immerse in boiling trichloroethylene (TCE) for 3 min.
  **2.** Immerse in boiling acetone for 3 min.
  **3.** Immerse in boiling methyl alcohol for 3 min.
  **4.** Wash in DI water for 3 min.

**B.** Removal of Residual Organic/Ionic Contamination
  **1.** Immerse in a (5:1:1) solution of $H_2O$–$NH_4OH$–$H_2O_2$; heat solution to 75–80 °C and hold for 10 min.
  **2.** Quench the solution under running DI water for 1 min.
  **3.** Wash in DI water for 5 min.

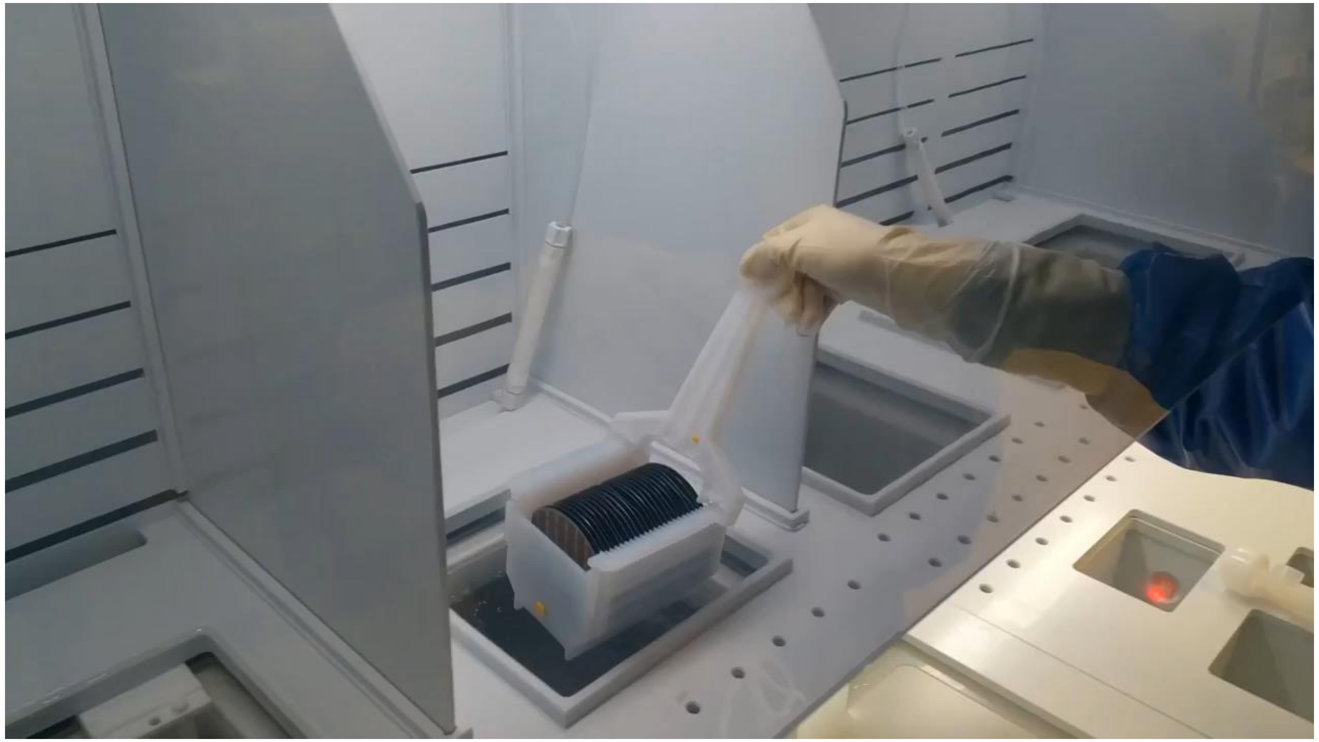
**C.** Hydrous Oxide Removal
  **1.** Immerse in a (1:50) solution of HF–$H_2O$ for 15 sec.
  **2.** Wash in running DI water with agitation for 30 sec.

**D.** Heavy Metal Clean
  **1.** Immerse in a (6:1:1) solution of $H_2O$–HCl–$H_2O_2$ for 10 min at a temperature of 75–80 °C.
  **2.** Quench the solution under running DI water for 1 min.
  **3.** Wash in running DI water for 20 min.

R. C. Jaeger, Introduction to microelectronic fabrication, 2nd Edition.

# Piranha cleaning

- ✓ A piranha solution is used to remove organic residues from substrates.
- ✓ The piranha solution is made of a 3:1 mixture of concentrated sulfuric acid ($H_2SO_4$) with hydrogen peroxide ($H_2O_2$).



https://youtu.be/HiJNI8k1doc

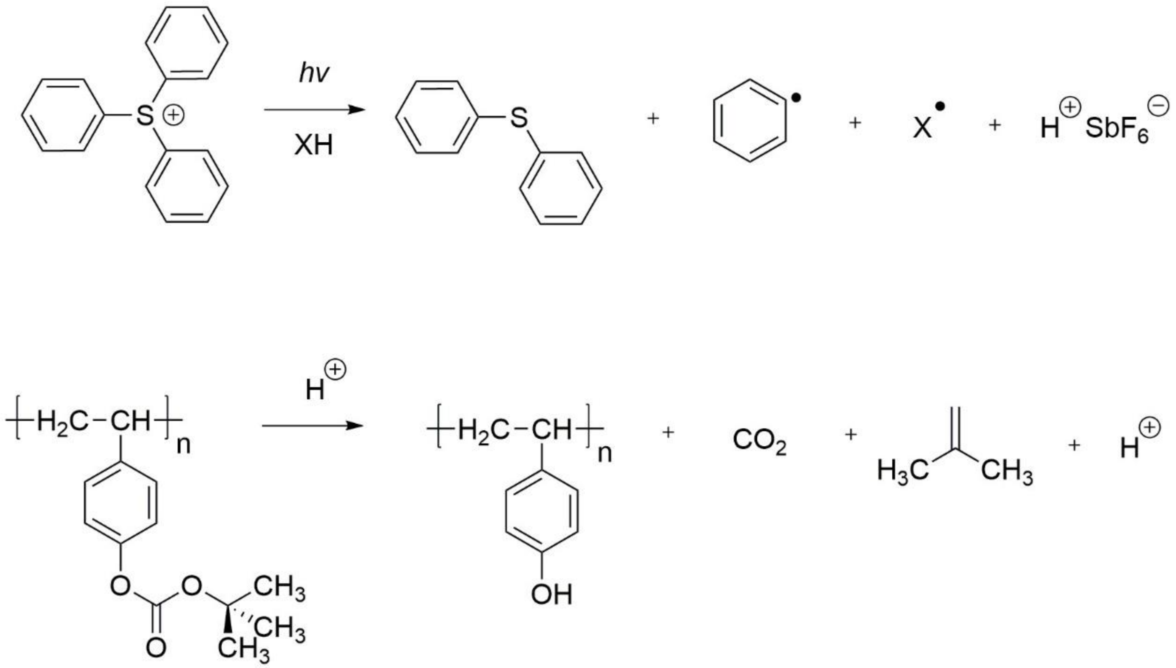
# Photolithography

- Clean wafers
- Coat with photoresist
- Soft bake
- Align masks
- Exposure pattern
- Develop photoresist
- Hard bake
- Etch a window

# Coat with photoresist: Photoresist

✓ A photoresist is a light-sensitive material used in photolithography to form a patterned coating on a surface.

✓ A positive photoresist is a type of photoresist in which the portion of the photoresist that is exposed to light becomes soluble to the photoresist developer. (negative photoresist)

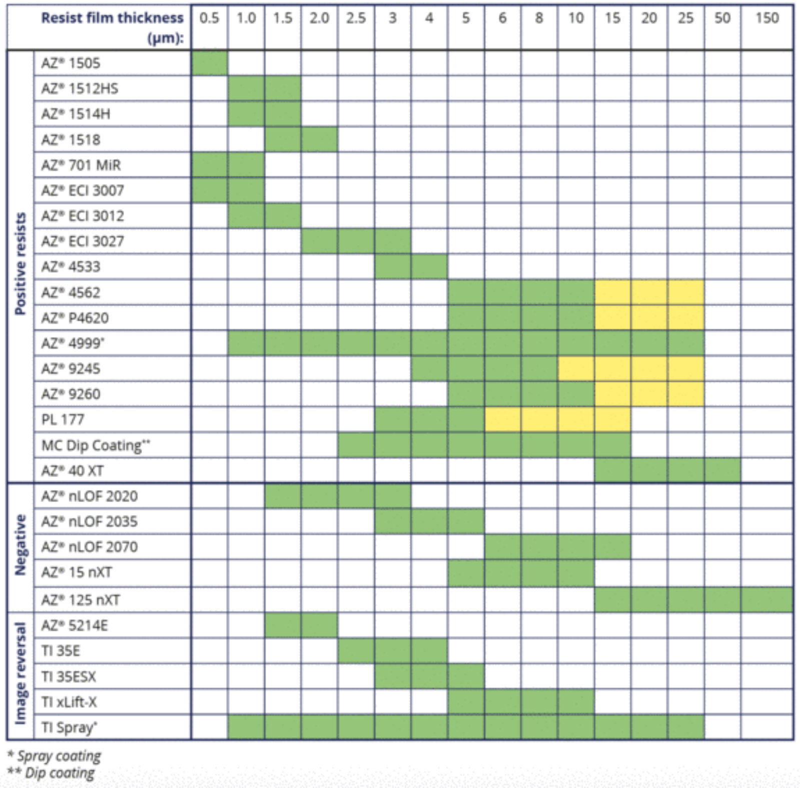


A positive photoresist example : its solubility would change by the photogenerated acid.
The acid deprotects the *tert*-butoxycarbonyl (t-BOC), <u>inducing the resist from alkali insoluble to alkali soluble</u>.

# Coat with photoresist

- ✓ Adhesion promoter such as hexamethyldisilazane (HMDS) provides good photoresist adhesion to a variety of films.
- ✓ The actual thickness of the resist depends on its viscosity and is inversely proportional to the square root of the spinning speed. Generally, the last two digits of the photoresist name indicate the film thickness attained by spin coating at 4000 rpm.

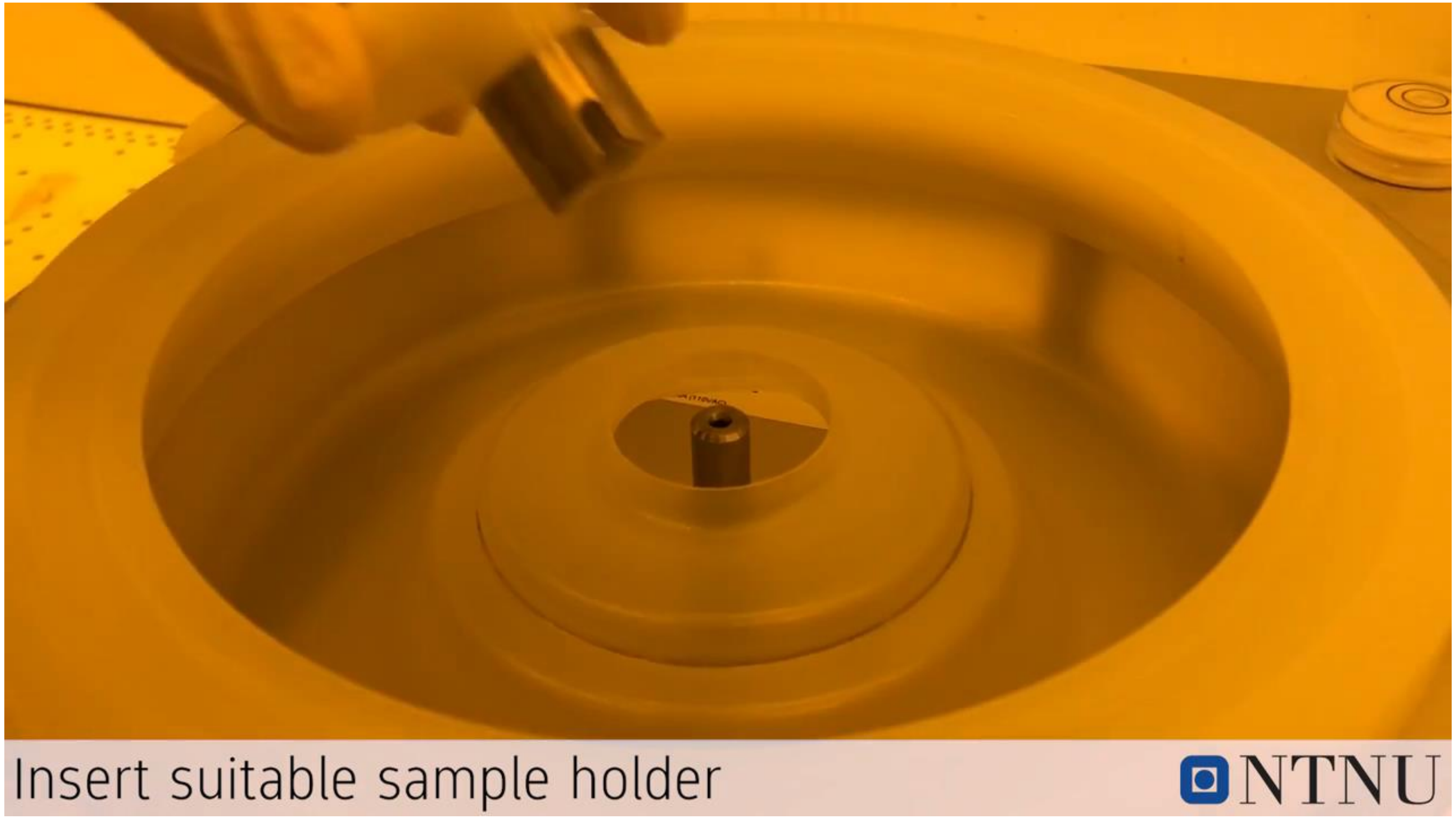
MicroChemicals



|  | Resist film thickness (µm): | 0.5 | 1.0 | 1.5 | 2.0 | 2.5 | 3 | 4 | 5 | 6 | 8 | 10 | 15 | 20 | 25 | 50 | 150 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Positive resists | AZ® 1505 | 🟩 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  | AZ® 1512HS |  | 🟩 | 🟩 |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  | AZ® 1514H |  | 🟩 | 🟩 |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  | AZ® 1518 |  |  | 🟩 | 🟩 |  |  |  |  |  |  |  |  |  |  |  |  |
|  | AZ® 701 MiR | 🟩 | 🟩 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  | AZ® ECI 3007 | 🟩 | 🟩 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  | AZ® ECI 3012 |  | 🟩 | 🟩 |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  | AZ® ECI 3027 |  |  |  | 🟩 | 🟩 | 🟩 |  |  |  |  |  |  |  |  |  |  |
|  | AZ® 4533 |  |  |  |  |  | 🟩 | 🟩 |  |  |  |  |  |  |  |  |  |
|  | AZ® 4562 |  |  |  |  |  |  |  | 🟩 | 🟩 | 🟩 | 🟩 | 🟨 | 🟨 | 🟨 |  |  |
|  | AZ® P4620 |  |  |  |  |  |  |  | 🟩 | 🟩 | 🟩 | 🟩 | 🟨 | 🟨 | 🟨 |  |  |
|  | AZ® 4999* |  | 🟩 | 🟩 | 🟩 | 🟩 | 🟩 | 🟩 | 🟩 | 🟩 | 🟩 | 🟩 | 🟩 | 🟩 | 🟩 |  |  |
|  | AZ® 9245 |  |  |  |  |  |  | 🟩 | 🟩 | 🟩 | 🟩 | 🟨 | 🟨 | 🟨 | 🟨 |  |  |
|  | AZ® 9260 |  |  |  |  |  |  |  | 🟩 | 🟩 | 🟩 | 🟩 | 🟨 | 🟨 | 🟨 |  |  |
|  | PL 177 |  |  |  |  |  | 🟩 | 🟩 | 🟩 | 🟨 | 🟨 | 🟨 | 🟨 |  |  |  |  |
|  | MC Dip Coating** |  |  |  |  | 🟩 | 🟩 | 🟩 | 🟩 | 🟩 | 🟩 | 🟩 | 🟩 |  |  |  |  |
|  | AZ® 40 XT |  |  |  |  |  |  |  |  |  |  |  | 🟩 | 🟩 | 🟩 | 🟩 |  |
| Negative | AZ® nLOF 2020 |  |  | 🟩 | 🟩 | 🟩 | 🟩 |  |  |  |  |  |  |  |  |  |  |
|  | AZ® nLOF 2035 |  |  |  |  |  | 🟩 | 🟩 | 🟩 |  |  |  |  |  |  |  |  |
|  | AZ® nLOF 2070 |  |  |  |  |  |  |  |  | 🟩 | 🟩 | 🟩 | 🟩 |  |  |  |  |
|  | AZ® 15 nXT |  |  |  |  |  |  |  | 🟩 | 🟩 | 🟩 | 🟩 |  |  |  |  |  |
|  | AZ® 125 nXT |  |  |  |  |  |  |  |  |  |  |  | 🟩 | 🟩 | 🟩 | 🟩 | 🟩 |
| Image reversal | AZ® 5214E |  |  | 🟩 | 🟩 |  |  |  |  |  |  |  |  |  |  |  |  |
|  | TI 35E |  |  |  |  | 🟩 | 🟩 | 🟩 |  |  |  |  |  |  |  |  |  |
|  | TI 35ESX |  |  |  |  |  | 🟩 | 🟩 | 🟩 |  |  |  |  |  |  |  |  |
|  | TI xLift-X |  |  |  |  |  |  |  | 🟩 | 🟩 | 🟩 | 🟩 |  |  |  |  |  |
|  | TI Spray* |  | 🟩 | 🟩 | 🟩 | 🟩 | 🟩 | 🟩 | 🟩 | 🟩 | 🟩 | 🟩 | 🟩 | 🟩 | 🟩 |  |  |

** Spray coating*
*** Dip coating*

# Coat with photoresist



https://youtu.be/WAFE6pZBT9c

# Photolithography

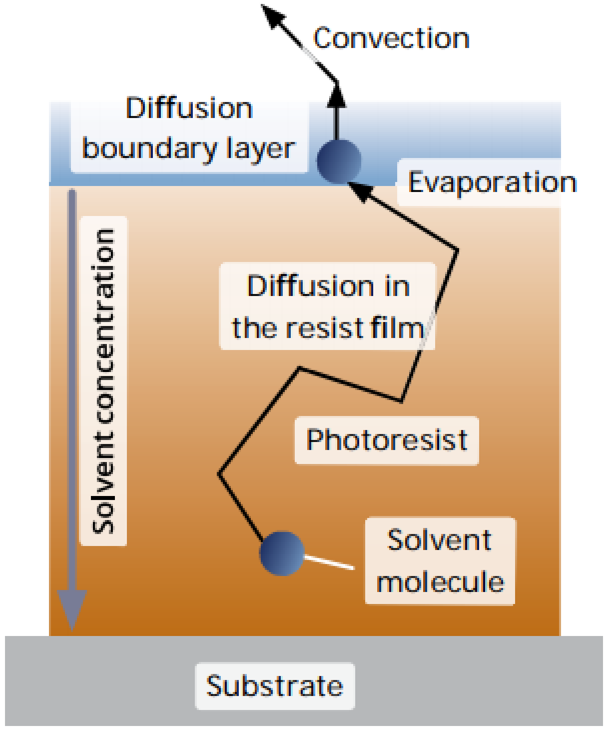
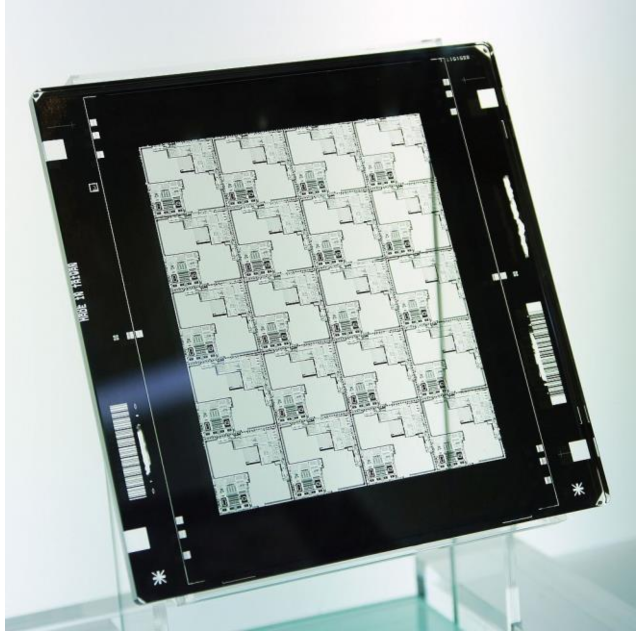


Fig. 64: To leave the resist film, a solvent molecule must first diffuse on the resist surface, evaporate, diffuse through the diffusion boundary layer above the resist surface and ultimately be carried away by the air stream.

- Oven at 80 ℃, 5 min

- Clean wafers
- Coat with photoresist
- Soft bake
- Align masks
- Exposure pattern
- Develop photoresist
- Hard bake
- Etch a window

# Photolithography



- Power
- Exposure duration

Clean wafers

Coat with photoresist

Soft bake

Align masks

Exposure pattern

Develop photoresist

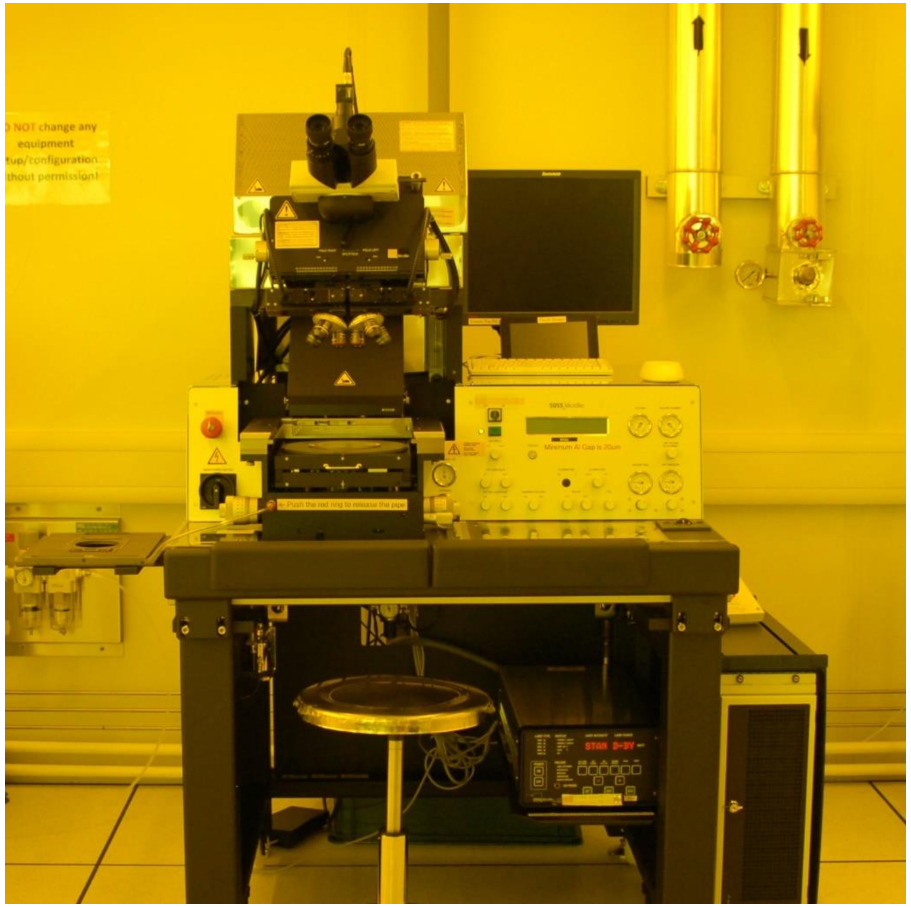
Hard bake

Etch a window

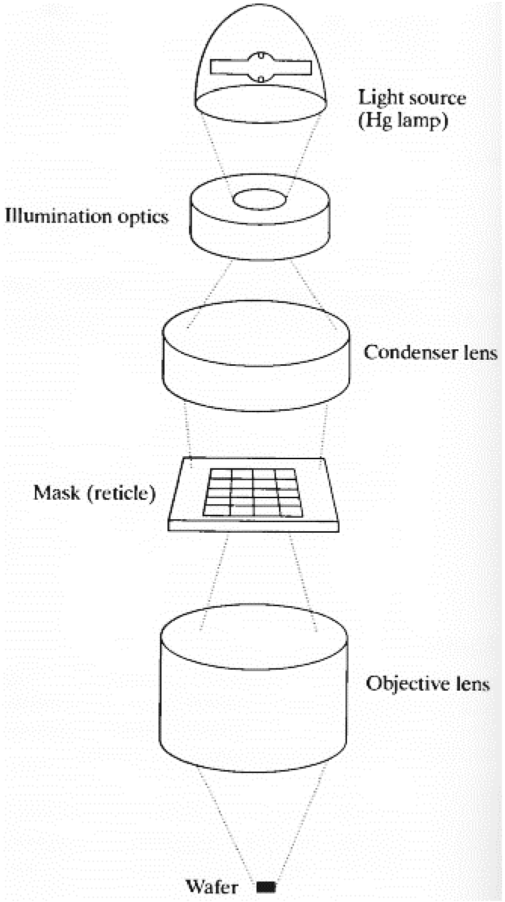
Remove photoresist

# Align mask / Exposure pattern: Aligner

MA6 Mask Aligner



Light source: 350W UV light
Resolution: < 0.8 um
Alignment accuracy: < ± 0.5um
up to 4” round wafer



The minimum feature size ~ $F = 0.5\,\frac{\lambda}{NA}$

R. C. Jaeger, Introduction to microelectronic fabrication, 2nd Edition.

# Photolithography

Clean wafers

Coat with photoresist

Soft bake

Align masks

Exposure pattern

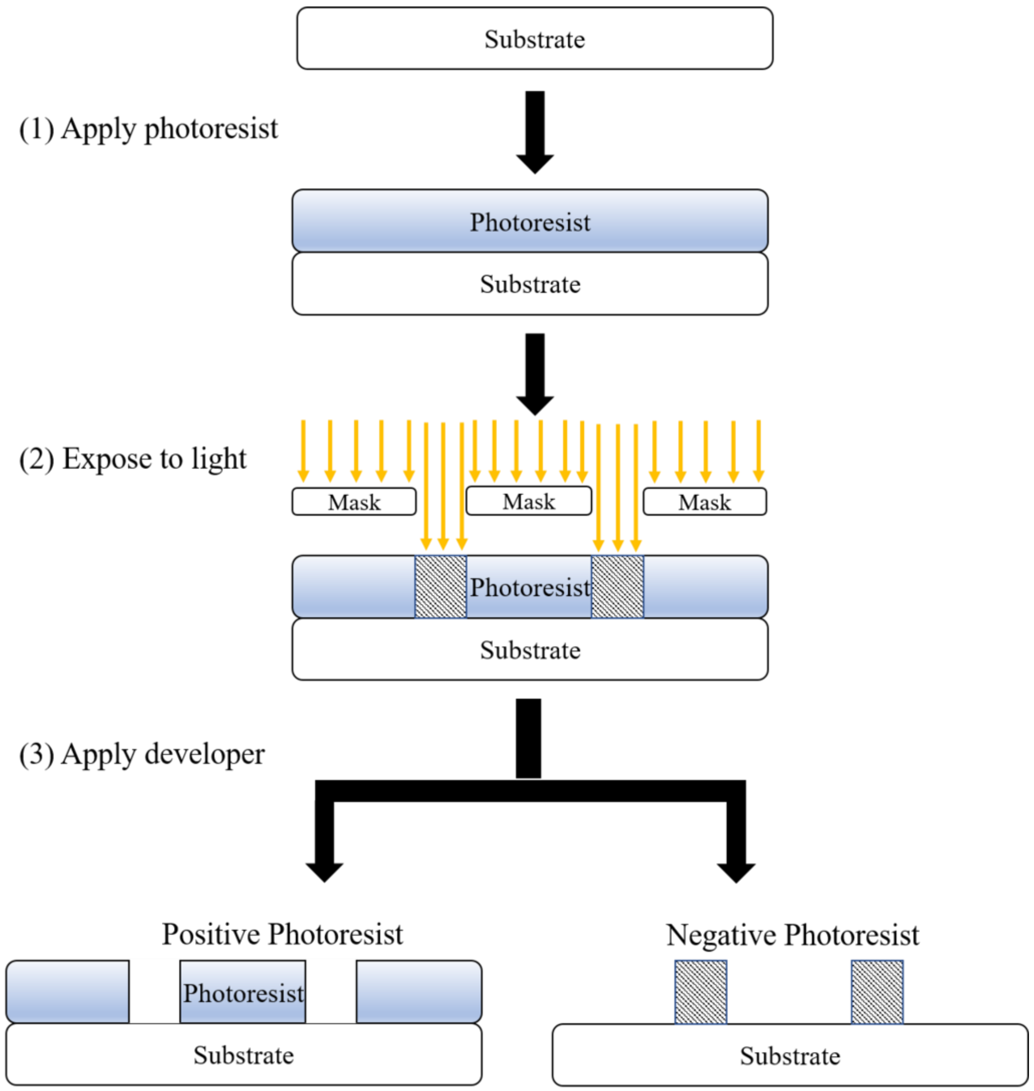
Develop photoresist

Hard bake

Etch a window

Remove photoresist

# Develop photoresist



# Photolithography

Clean wafers

Coat with photoresist

Soft bake

Align masks

Exposure pattern

Develop photoresist

Hard bake

Etch a window

Remove photoresist

ICP-RIE
1000 Å etching
Alpha step or ellipsometer

# Etch a window
# : Reactive ion etching (RIE)

- ✓ RIE is an etching technology. RIE is a type of dry etching. RIE uses chemically reactive plasma to remove material deposited on wafers. High-energy ions from the plasma attack the wafer surface and react with it.

- ✓ Etching occurs through a combination of the chemical reaction and momentum transfer from the etching species and is highly anisotropic.

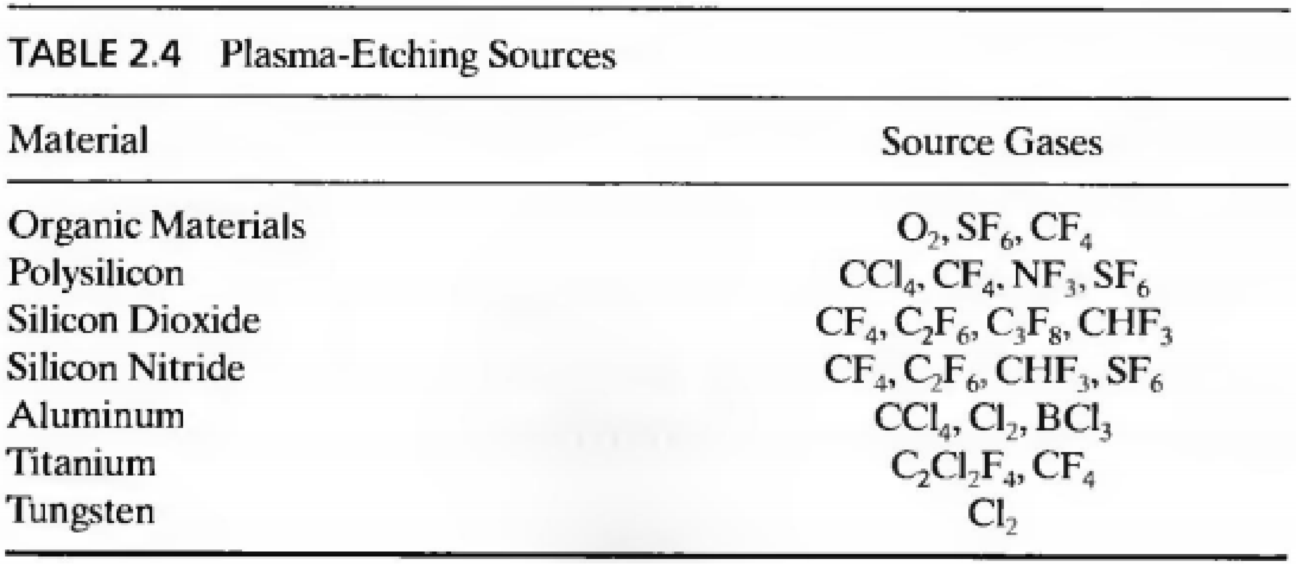


**TABLE 2.4** Plasma-Etching Sources

| Material | Source Gases |
|---|---|
| Organic Materials | $O_2$, $SF_6$, $CF_4$ |
| Polysilicon | $CCl_4$, $CF_4$, $NF_3$, $SF_6$ |
| Silicon Dioxide | $CF_4$, $C_2F_6$, $C_3F_8$, $CHF_3$ |
| Silicon Nitride | $CF_4$, $C_2F_6$, $CHF_3$, $SF_6$ |
| Aluminum | $CCl_4$, $Cl_2$, $BCl_3$ |
| Titanium | $C_2Cl_2F_4$, $CF_4$ |
| Tungsten | $Cl_2$ |

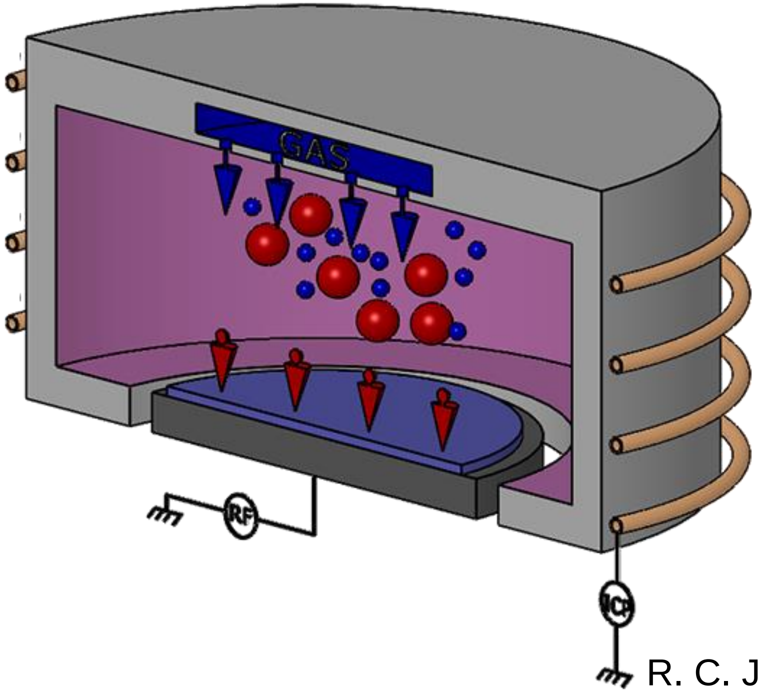
R. C. Jaeger, Introduction to microelectronic fabrication, 2nd Edition.

# Etch a window
# : Inductively Coupled Plasma-Reactive ion etching (ICP-RIE)

- ✓ ICP-RIE etching is based on the use of an inductively coupled plasma source.

- ✓ The ICP source generates a high-density plasma due to inductive coupling between the RF antenna and the plasma.

- ✓ The antenna, located in the plasma generation region, creates an alternating RF magnetic field and induces RF electric fields, which energize electrons that participate in the ionization of gas molecules and atoms at low pressure.



R. C. Jaeger, Introduction to microelectronic fabrication, 2nd Edition.

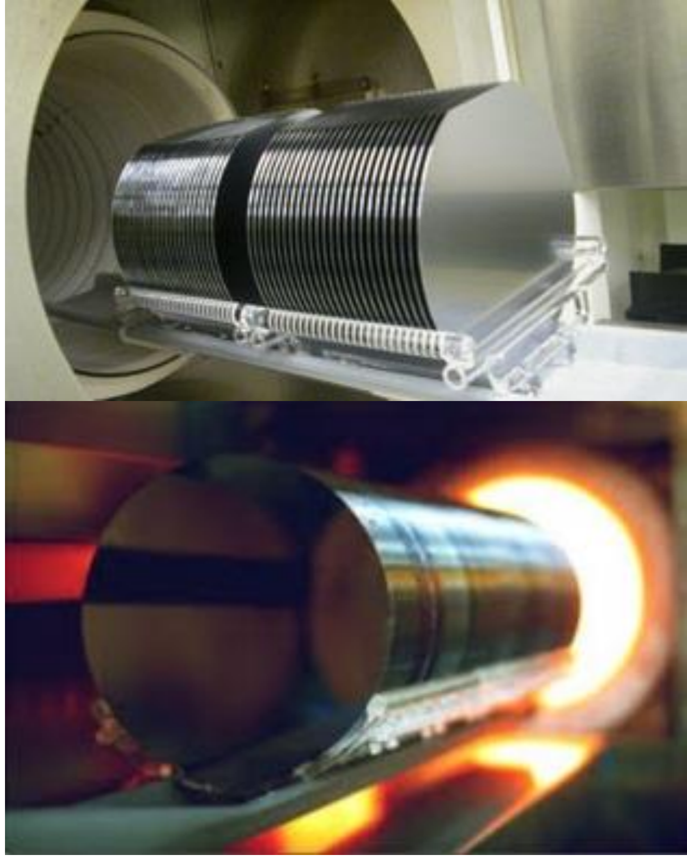
# 2. Gate Dry Oxidation

**1. Active (Si channel) etching**

**2. Gate dry oxidation**

150 Å (±10%)

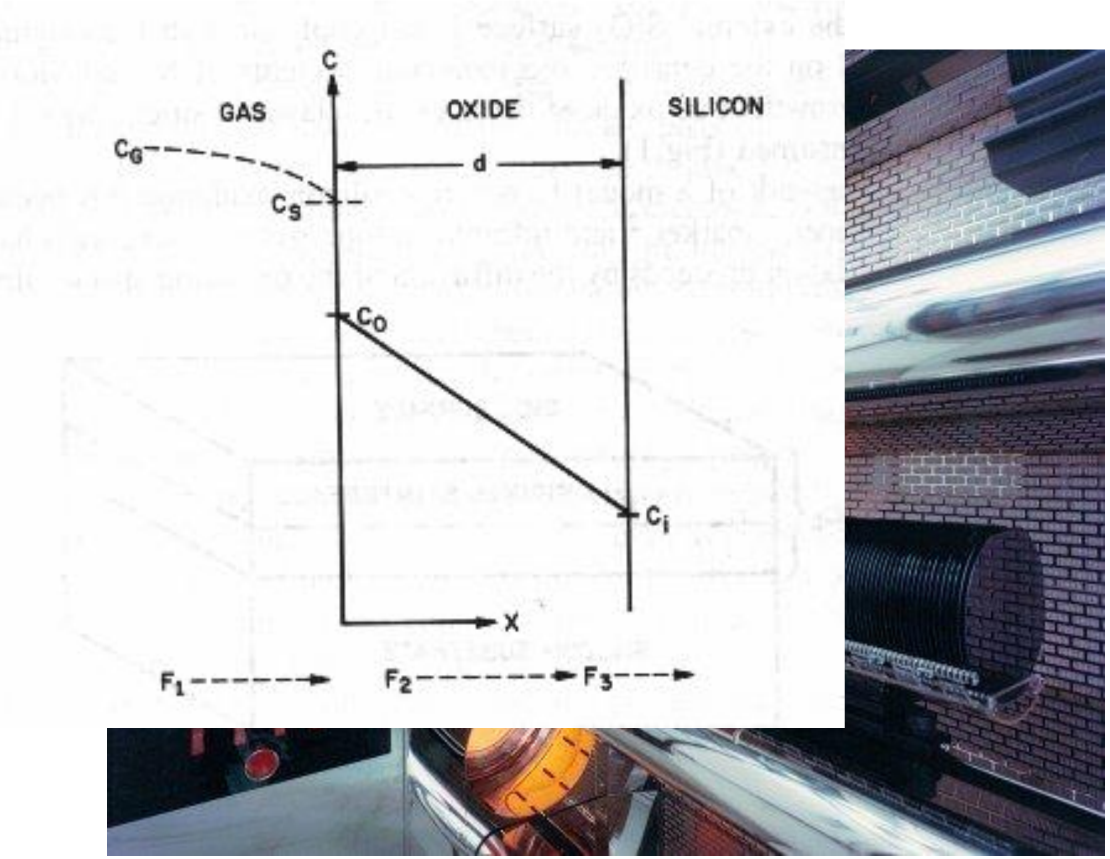
# Thermal oxidation of Silicon



✓ Upon exposure to oxygen, the surface of a silicon wafer oxidizes to form silicon dioxide. This native silicon dioxide film is high quality electrical insulator and can be used as a barrier material during impurity deposition. The extreme purity and perfection of the Si/$SiO_2$ interface is the ultimate reason why silicon has been #1 semiconductor for microelectronics.

# Thermal oxidation of Silicon

Deal and Grove’s model



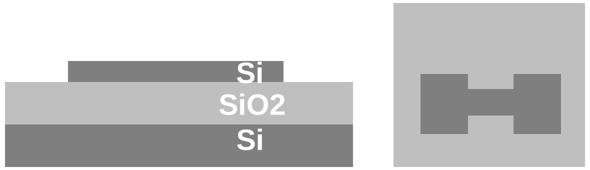
- ✓ Thermal oxidation of silicon is achieved by heating the wafer to a high temperature, typically 900 to 1200 ℃ in an atmosphere containing either pure oxygen(dry).
- ✓ Oxygen move (diffuse) easily through silicon dioxide at these high temperature. Oxygen arriving at the silicon surface can then combine with silicon to form silicon dioxide.
- ✓ Silicon is consumed as the oxide grows, and the resulting oxide expands during growth.

Control factors: temperature, pressure, crystal direction

B. E. Deal, A. S. Grove, *J. Appl. Phys.* 36, 3770 (1965).

# 3. Electrode Deposition

**1. Active (Si channel) etching**

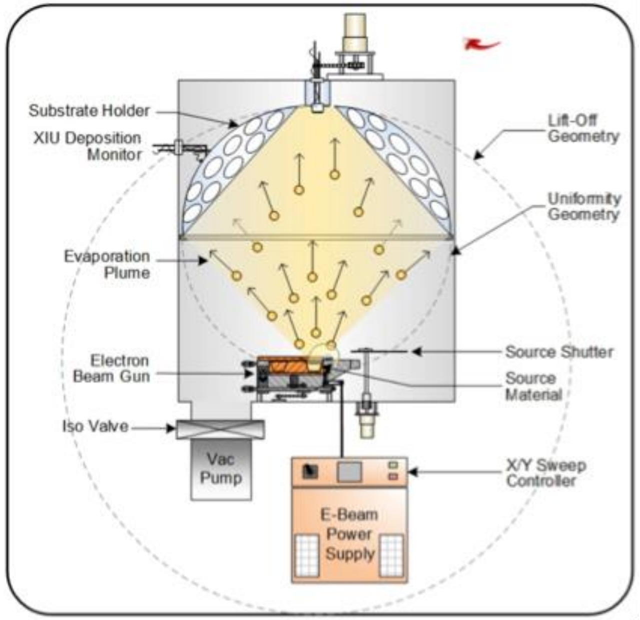


**2. Gate dry oxidation**

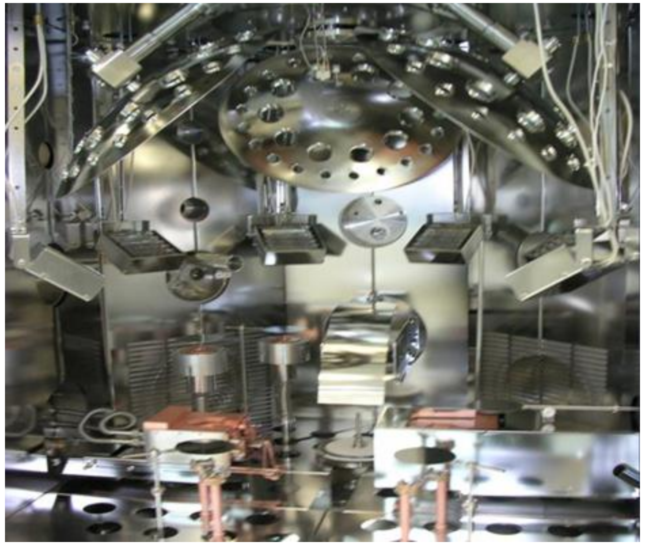
**3. Electrode deposition**

- Photolithography
- Metallic film deposition

# Metallic film deposition
# : Electron-beam evaporation



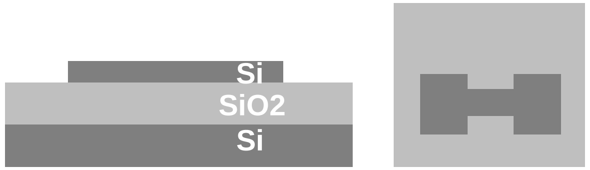
Lift-off process



- ✓ A high-intensity beam of electrons is focused on a source target containing the material to be evaporated. The energy from the electron beam melts a region of the target.
- ✓ Material evaporates from the source and covers the silicon wafers with a thin layer.

# 4. SiO2 cap ox.

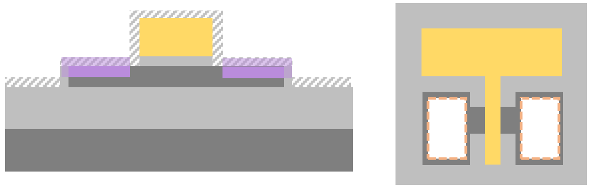
**1. Active (Si channel) etching**



**2. Gate dry oxidation**

**3. Electrode deposition**

**4. SiO2 cap ox.**

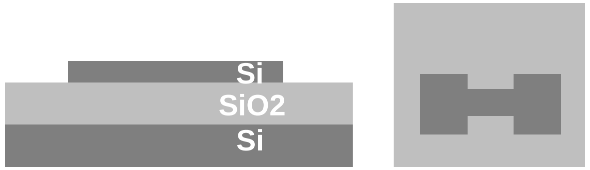


- Wet oxidation:

  a form of hydrothermal treatment using oxygen as the oxidizer.

# 5. Implantation

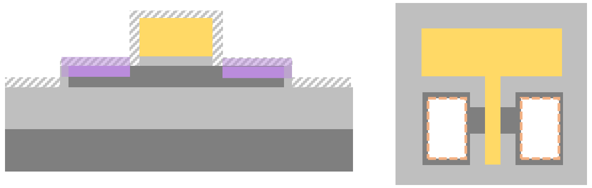
**1. Active (Si channel) etching**



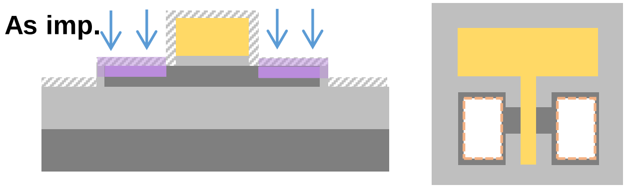
**2. Gate dry oxidation**

**3. Electrode deposition**

**4. SiO2 cap ox.**



**5. implantation**

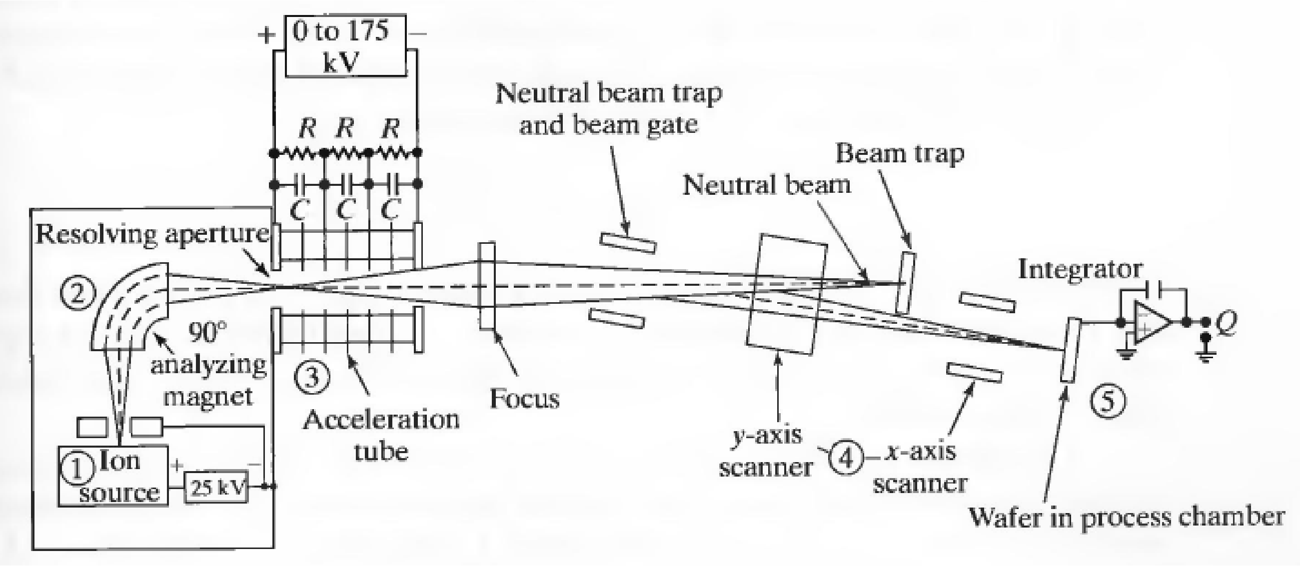


- Photolithography
- Implantation

  $As^+$
  100 keV
  3e15 for 500 Å $SiO_2$

# Implantation

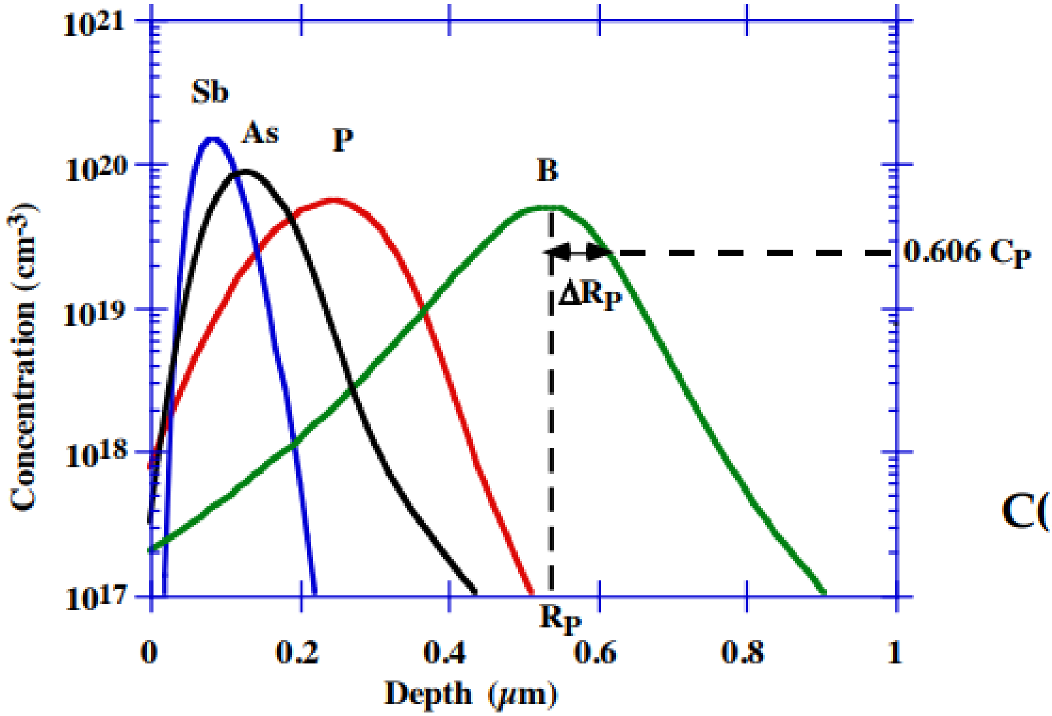
- ✓ Ion implantation introduces impurity atoms into the silicon wafer and has become a workhorse technology in modern IC fabrication.



Schematic drawing of a typical ion implanter showing (1) ion source, (2) mass spectrometer, (3) high-voltage accelerator column, (4) x- and y-axis deflection system, and (5) target chamber.

R. C. Jaeger, Introduction to microelectronic fabrication, 2nd Edition.

# Mathematical model for ion implantation

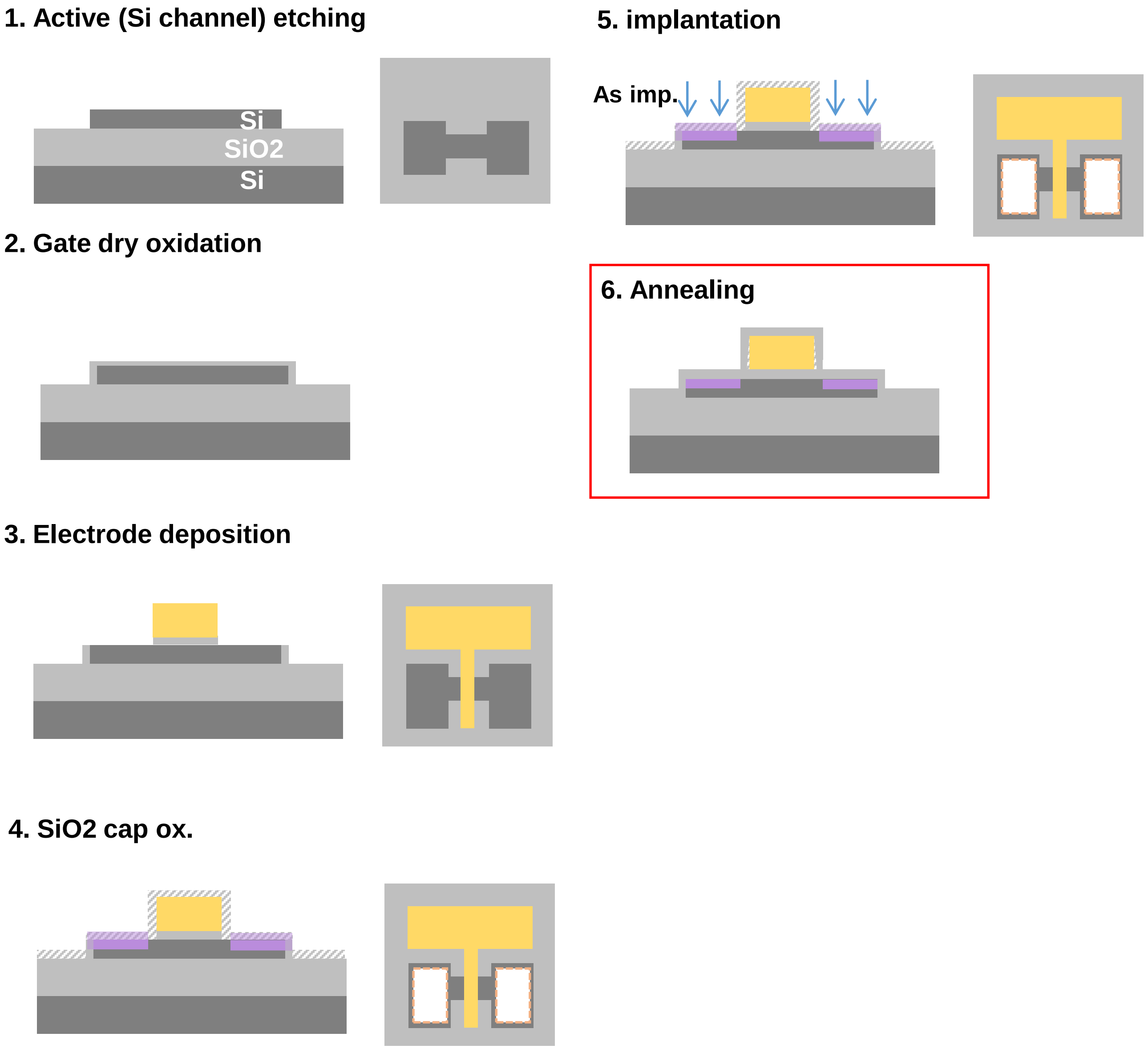


$$C(x) = C_P \exp\left(-\frac{(x - R_P)^2}{2\Delta R_P^2}\right)$$

- ✓ As an ion enters the surface of the wafer, it collides with atoms in the lattice and interacts with electrons in the crystal.

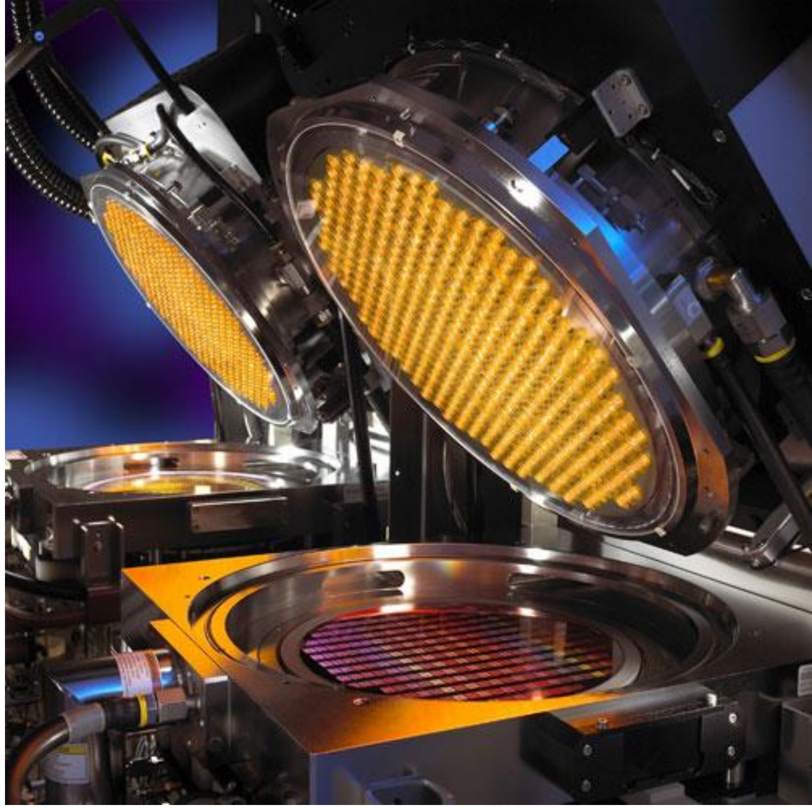
- ✓ Interaction with the crystal is a statistical process, and the implanted impurity profile can be approximated by the Gaussian distribution function.

# 6. Annealing



1. Active (Si channel) etching
2. Gate dry oxidation
3. Electrode deposition
4. SiO2 cap ox.
5. implantation
6. Annealing

# Rapid Thermal Annealing (RTA)



- ✓ Involves heating a material above its recrystallization temperature, maintaining a suitable temperature, and then cooling.

- ✓ In addition to removing the damage caused by the implantation, the annealing step is required to electrically activate the implanted impurities.

- ✓ In order to minimize diffusion of the shallow implanted profiles, rapid thermal annealing (RTA) was applied. The RTA can achieve the desired results with annealing times that range from a few minutes down to only a few seconds.

R. C. Jaeger, Introduction to microelectronic fabrication, 2nd Edition.

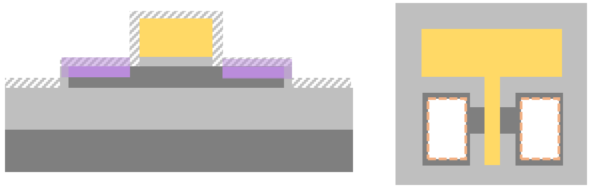
# 7. Cap ox etch/ passivation ox. dep

**1. Active (Si channel) etching**

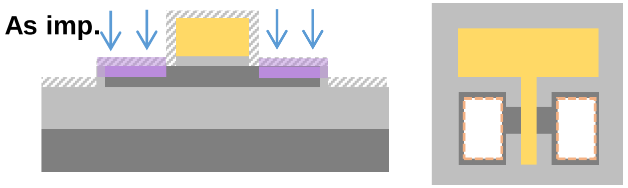
**2. Gate dry oxidation**

**3. Electrode deposition**

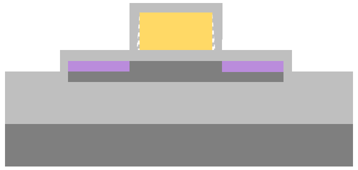
**4. SiO2 cap ox.**



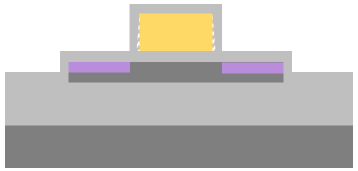
**5. implantation**



**6. Annealing**



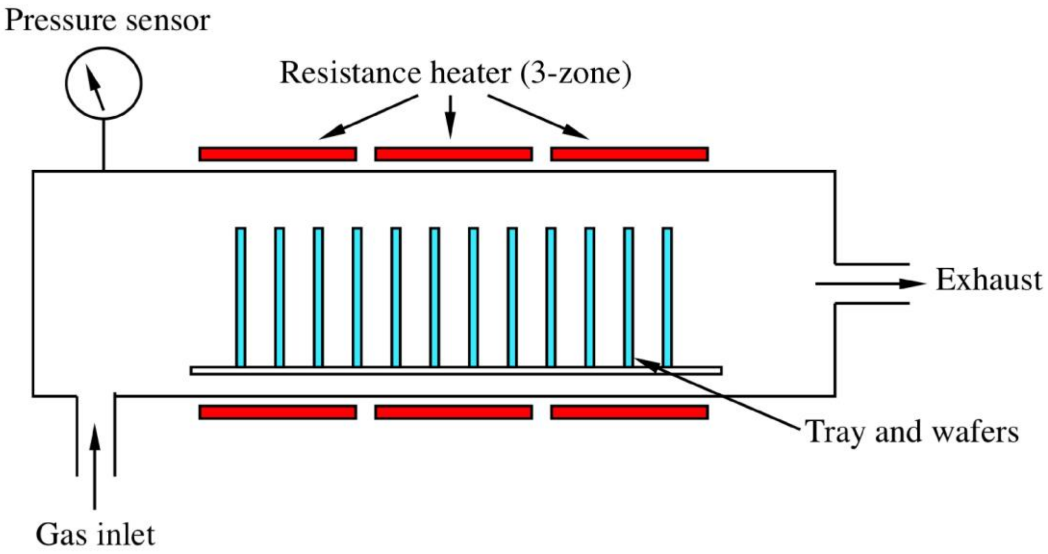
**7. Cap ox etch / passivation ox. dep**



- RIE
  $CHF_3$ 25 sccm
  $CF_4$ 5 sccm
  Ar 70 sccm
  RF 600 W
- Chemical vapor deposition

# Chemical vapor deposition (CVD)

- ✓ CVD forms thin films on the surface of a substrate by thermal decomposition or reaction of gaseous compounds.
- ✓ The desired material is deposited directly from the gas phase onto the surface of the substrate.
- ✓ Polysilicon, silicon dioxide, and silicon nitride



Chemical reaction in $SiO_2$ depostion

$$SiH_4 + O_2 \rightarrow SiO_2 + 2H_2$$

- A reaction between silane and oxygen between 300 and 500 ℃ is commonly used to deposit $SiO_2$.

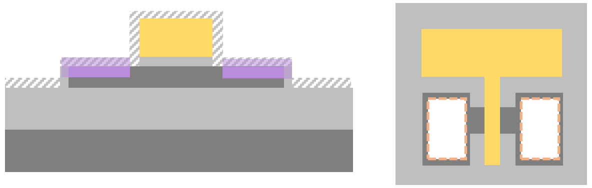
# 8. Contact hole etch / metal deposition

**1. Active (Si channel) etching**

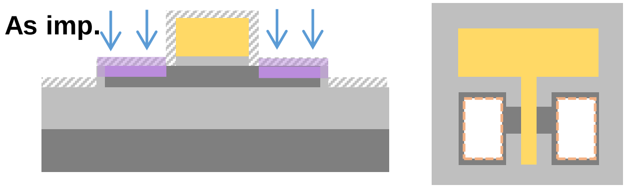
**2. Gate dry oxidation**

**3. Electrode deposition**

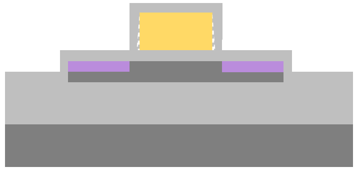
**4. SiO2 cap ox.**



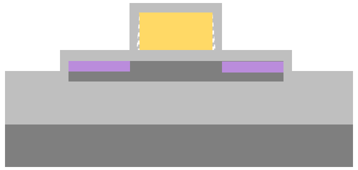
**5. implantation**



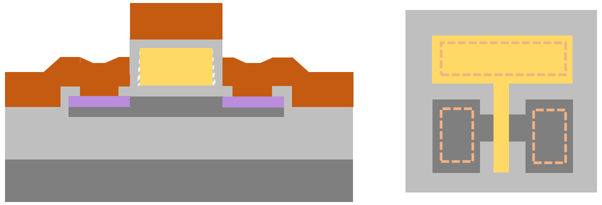
**6. Annealing**



**7. Cap ox etch / passivation ox. dep**



**8. S/D contact hole etch / (Ti/TiN/Al/TiN) deposition**



- Photolithography
- RIE
- Metal deposition

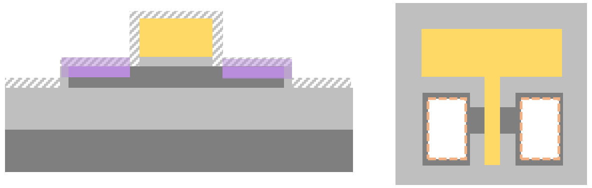
# 9. S/D contact metal etch

**1. Active (Si channel) etching**

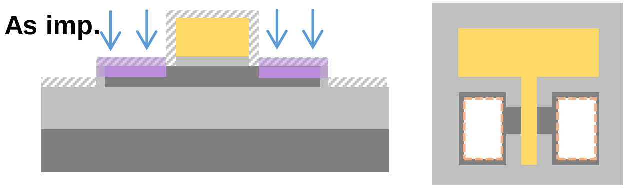
**2. Gate dry oxidation**

**3. Electrode deposition**

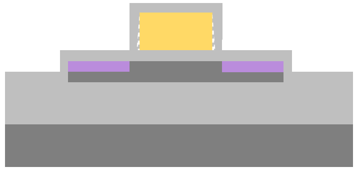
**4. SiO2 cap ox.**



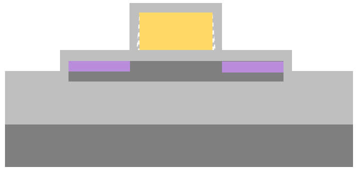
**5. implantation**



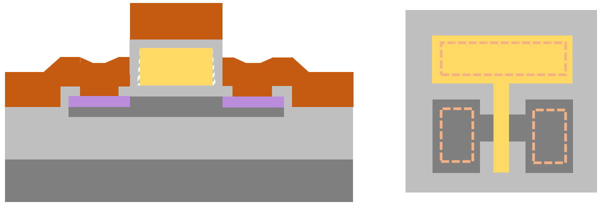
**6. Annealing**



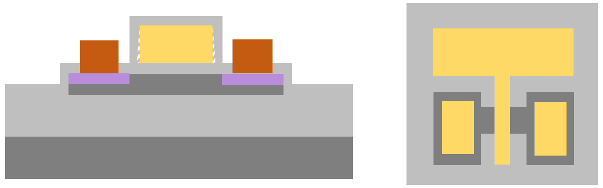
**7. Cap ox etch / passivation ox. dep**



**8. S/D contact hole etch / (Ti/TiN/Al/TiN) deposition**



**9. S/D contact metal etch**



- Photolithography
- RIE

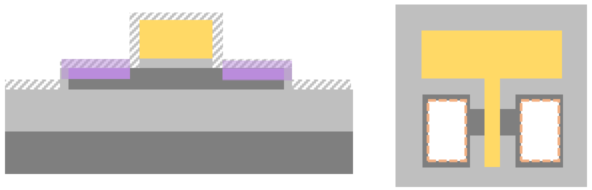
# 10. $H_2$ annealing

1. Active (Si channel) etching

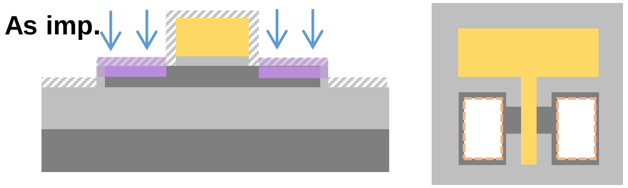
2. Gate dry oxidation

3. Electrode deposition

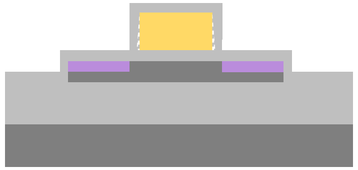
4. SiO2 cap ox.



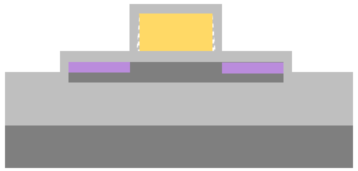
5. implantation



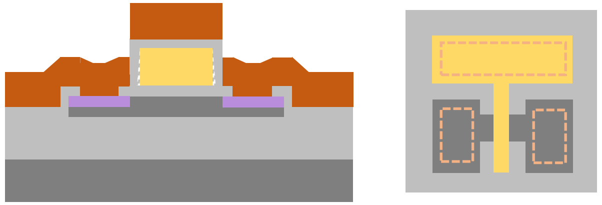
6. Annealing



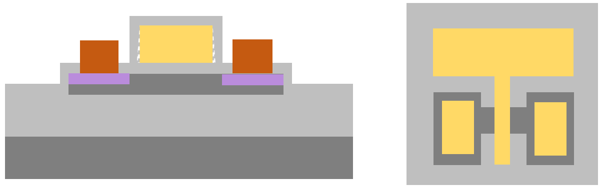
7. Cap ox etch / passivation ox. dep



8. S/D contact hole etch / (Ti/TiN/Al/TiN) deposition

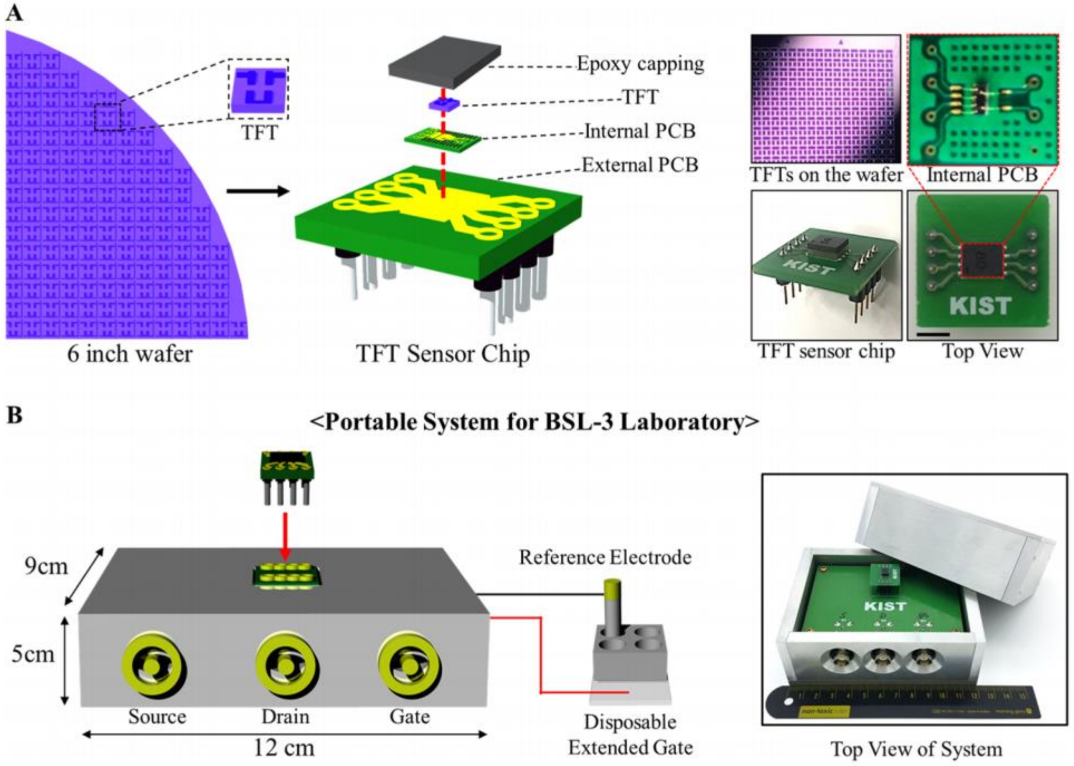


9. S/D contact metal etch

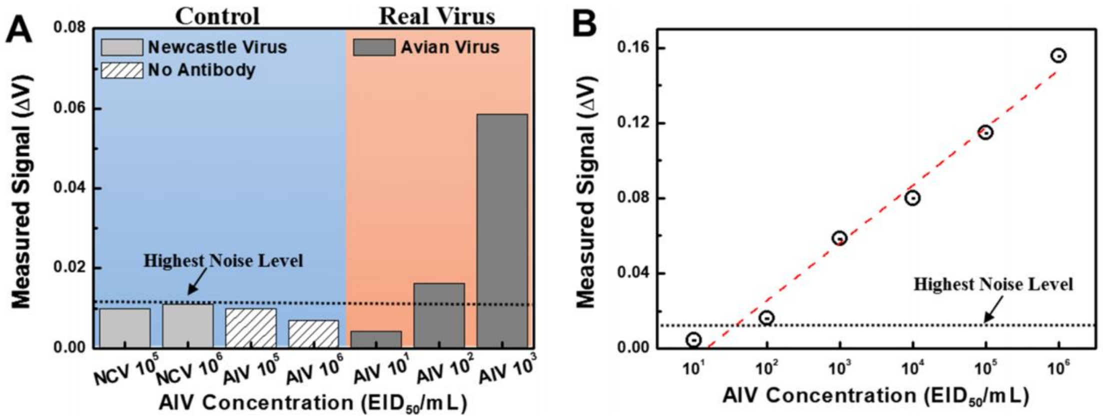


10. $H_2$ anneal

# Direct detection of highly pathogenic viruses from on-site samples



Overall schematic of the fully packaged biosensor



- The experimentally obtained limit of detection (LoD) is $10^2$ $EID_{50}$/mL.

- Egg Infective Dose$_{50}$ ($EID_{50}$)
  : One $EID_{50}$ unit is the amount of virus that will infect 50 percent of inoculated eggs.

- Current on-site methods have poor limits of $10^5$-$10^6$ $EID_{50}$/mL.

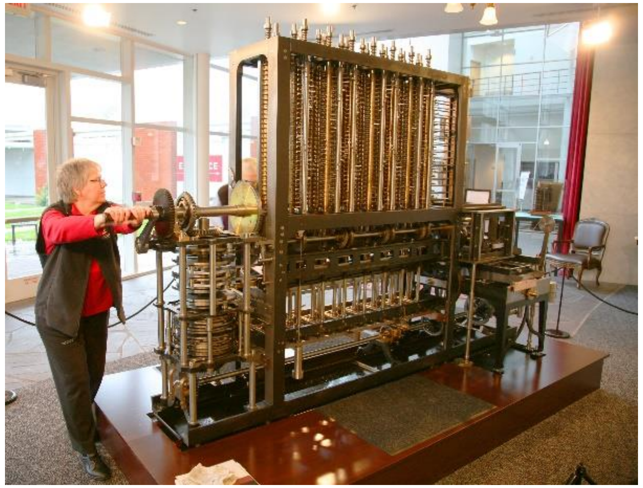
J. Choi *et al.*, *ACS nano 13*, 812 (2018)

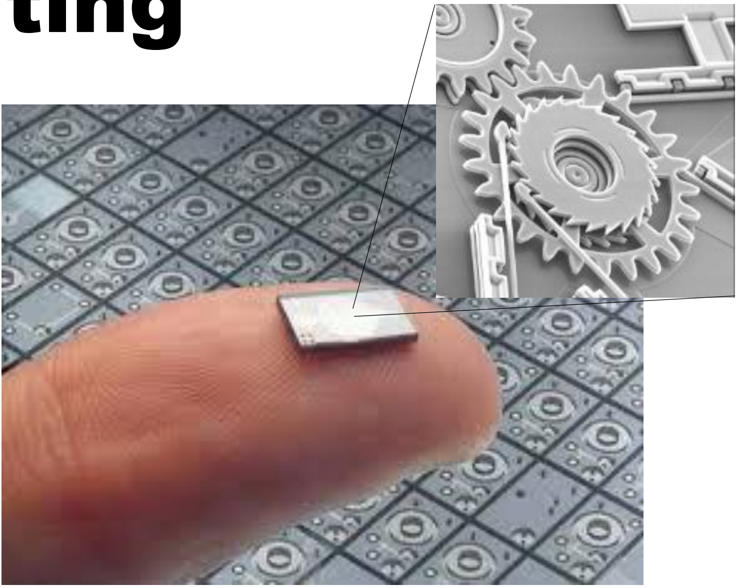
# Break Time

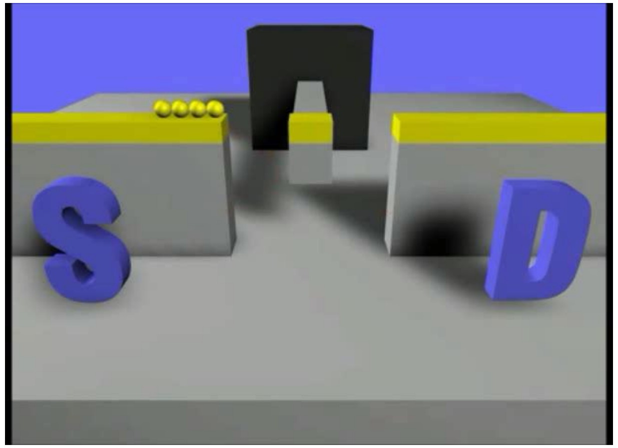
# Electron Shuttle as Nanoelectromechanical System (NEMS)

# Towards nanomechanical computing


Electromagnetic pulse(EMP) missile


Babbage’s mechanical computer (1921)

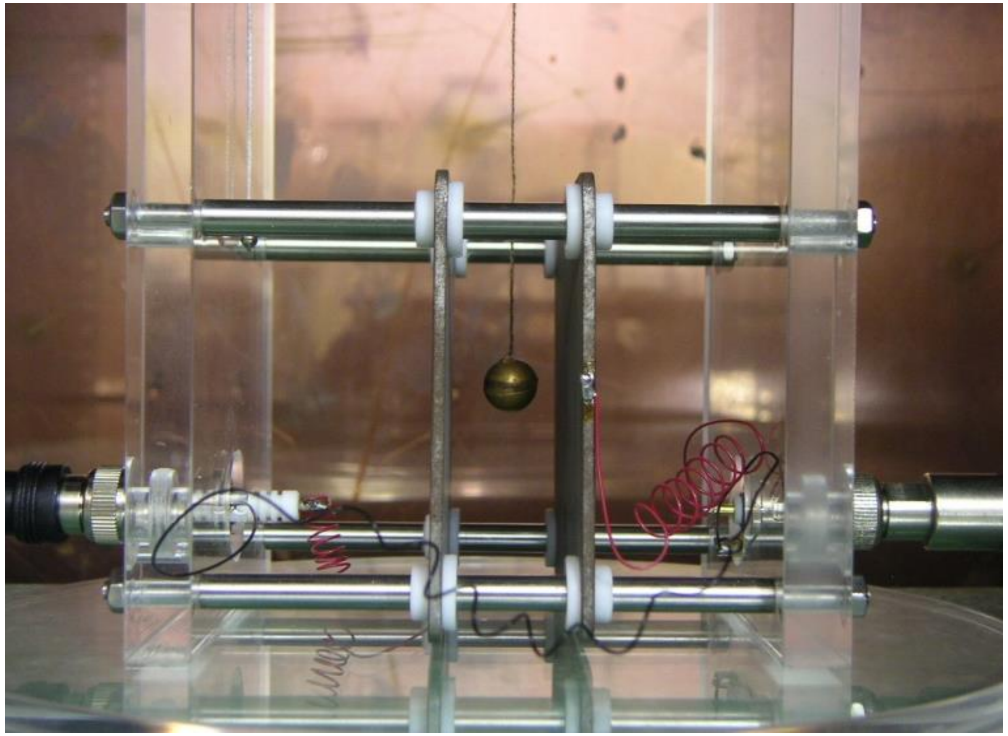

Micro-/Nano-electromechanical System (MEMS/NEMS)



Concept of electron shuttle

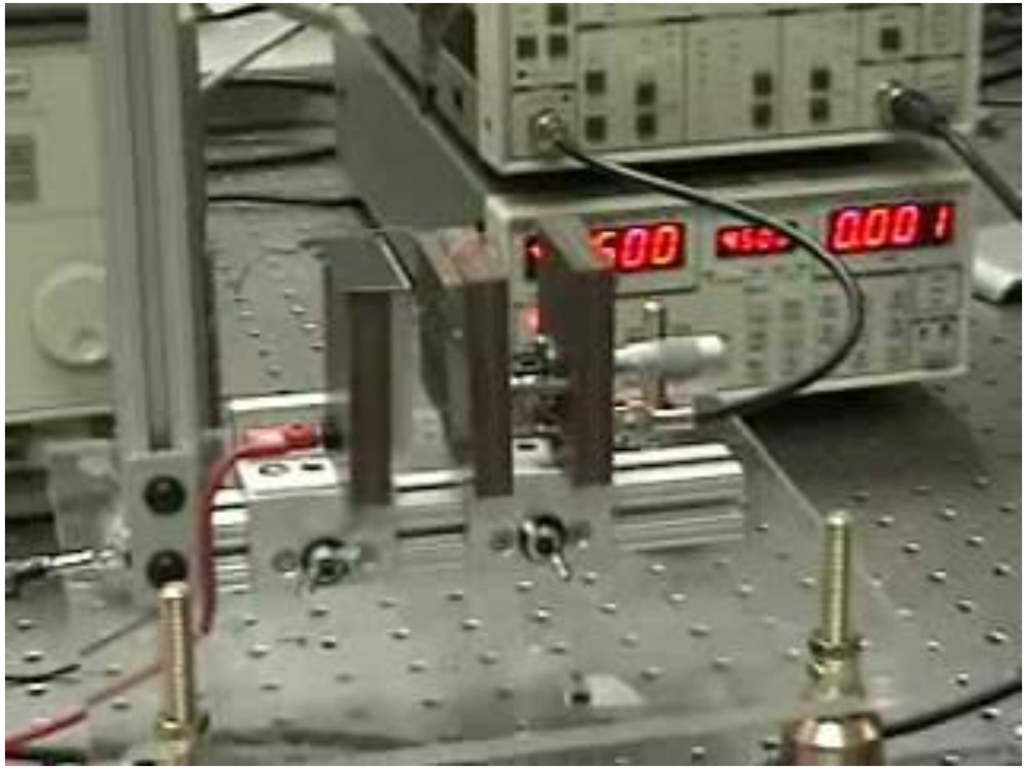
- ✓ Electrically isolated system
- ✓ High-speed operation with nanoscale resonators (up to a few GHz)
- ✓ Operable at high temperature (~200 ℃)

# Macro electron shuttle ver.1



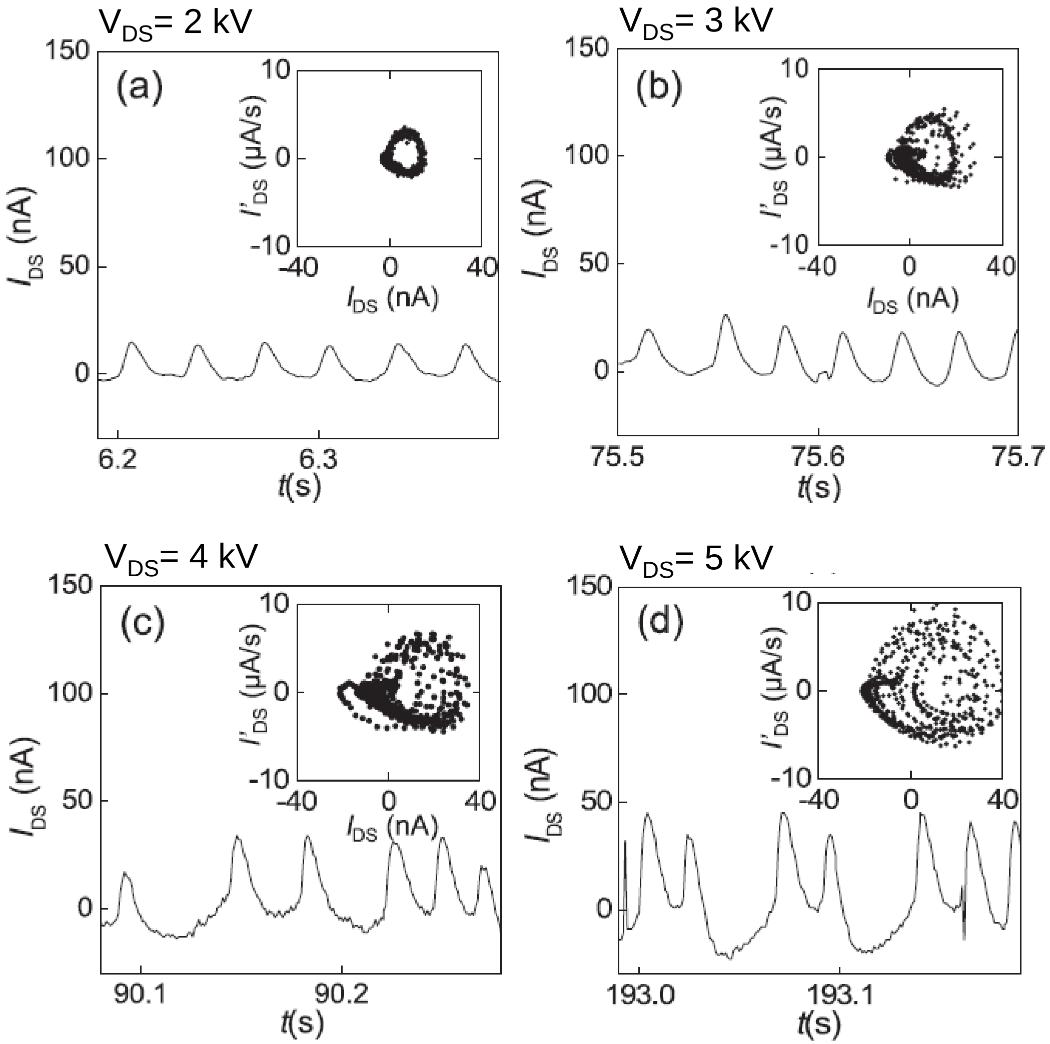
C. Kim *et al.*, *Appl. Phys. Lett.* 106, 061909 (2015)

# Macro electron shuttle ver.2



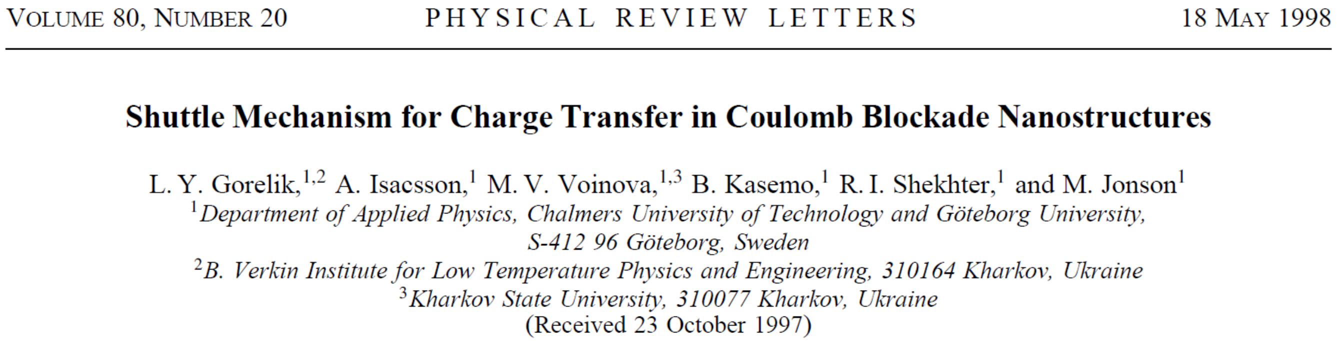
C. Kim *et al.*, *Appl. Phys. Lett.* 106, 061909 (2015)

# Current trace from the macro shuttle



C. Kim *et al.*, *Appl. Phys. Lett.* 106, 061909 (2015)

# Shuttle mechanism for charge transfer

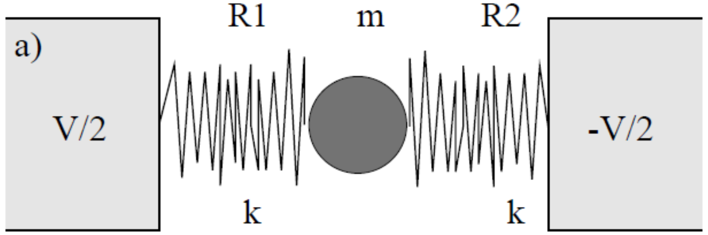


VOLUME 80, NUMBER 20 PHYSICAL REVIEW LETTERS 18 MAY 1998

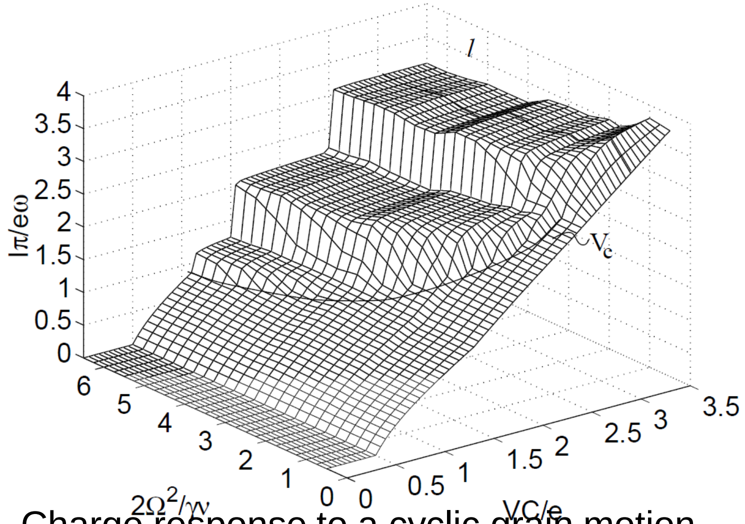
## Shuttle Mechanism for Charge Transfer in Coulomb Blockade Nanostructures

L. Y. Gorelik,[1,2] A. Isacsson,[1] M. V. Voinova,[1,3] B. Kasemo,[1] R. I. Shekhter,[1] and M. Jonson[1]
[1]*Department of Applied Physics, Chalmers University of Technology and Göteborg University, S-412 96 Göteborg, Sweden*
[2]*B. Verkin Institute for Low Temperature Physics and Engineering, 310164 Kharkov, Ukraine*
[3]*Kharkov State University, 310077 Kharkov, Ukraine*

(Received 23 October 1997)



Theory model for a shuttling system

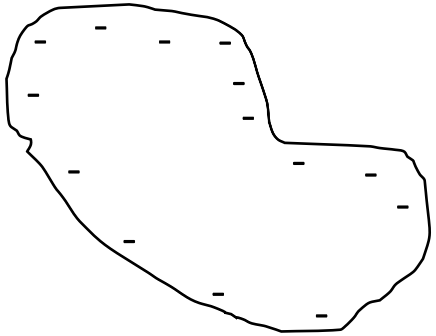


Charge response to a cyclic grain motion
The electrostatic force is at all times directed along the line of motion and thus accelerated the grain.
→ positive W → instability (self-excitation)

Current due to the proposed shuttle mechanism

L. Y. Gorelik *et al.*, *Phys. Rev. Lett.* 80, 4526 (1998)

# Coulomb Blockade



Isolated island: charge is quantized, Q=ne

Charging energy = addition energy : $E_C = \frac{e^2}{2C}$

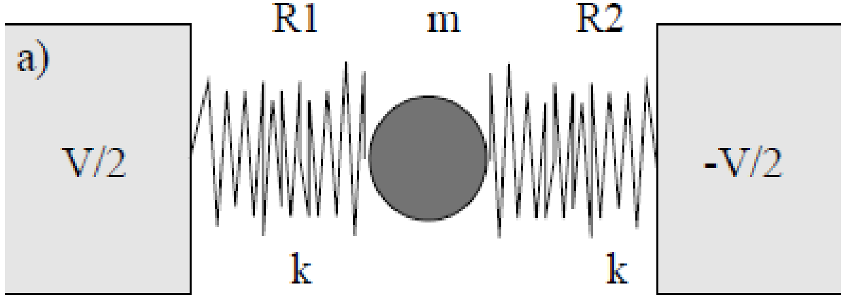
Versus level splitting δ: $L = 100nm\,; N_{atoms} = 10^9$

$$\delta \approx \frac{E_F}{N_{atoms}} \approx 10eV/N_{atoms} \approx 10^{-8}eV$$

$$E_C \approx 1meV$$

- ✓ If charging energy is not available (from external voltage sources or temperature), electron transport is blocked.

# Electron shuttles



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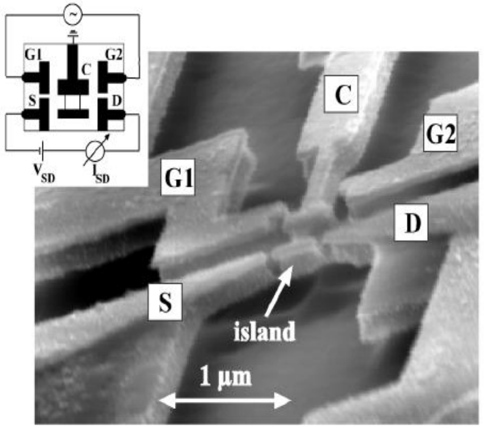
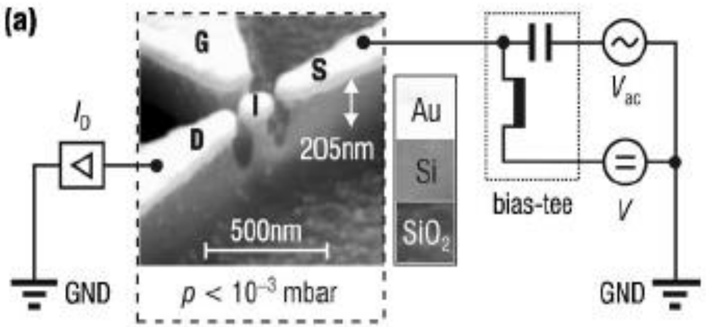


A. Erbe *et al.*, *Phys. Rev. Lett.* 87, 096106 (2001)



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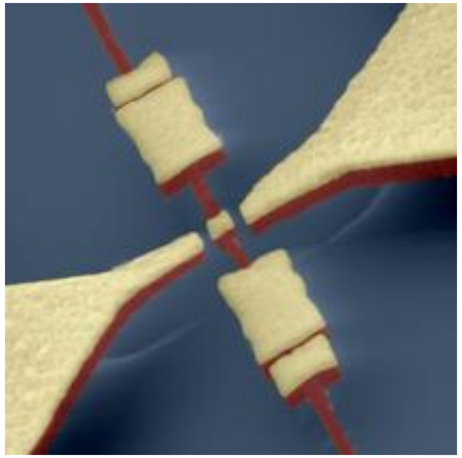
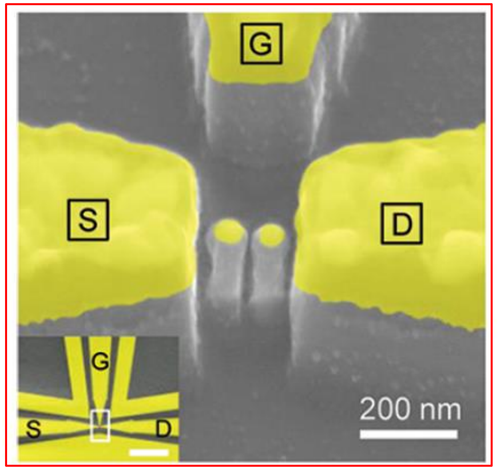


D. R. Koenig, *et al.*, *Nature Nanotech.* 3, 482 (2008)

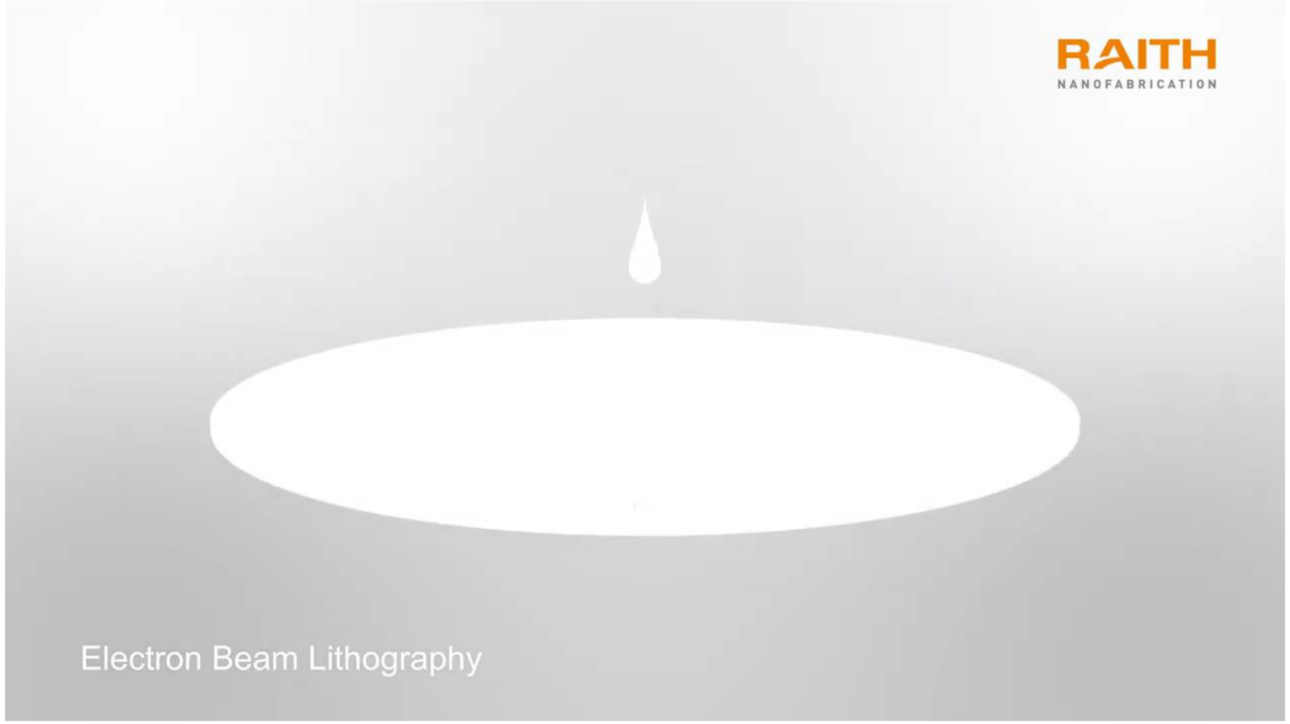


C. Kim *et al.*, *Phys. Rev. Lett.* 105, 067204 (2010)
C. Kim *et al.*, *Phys. Rev. Lett.* 105, 067204 (2013)

# Electron beam lithography

- ✓ Electron-beam lithography (EBL) is the practice of scanning a focused beam of electrons to draw custom shapes on a surface covered with an electron-sensitive film called a resist

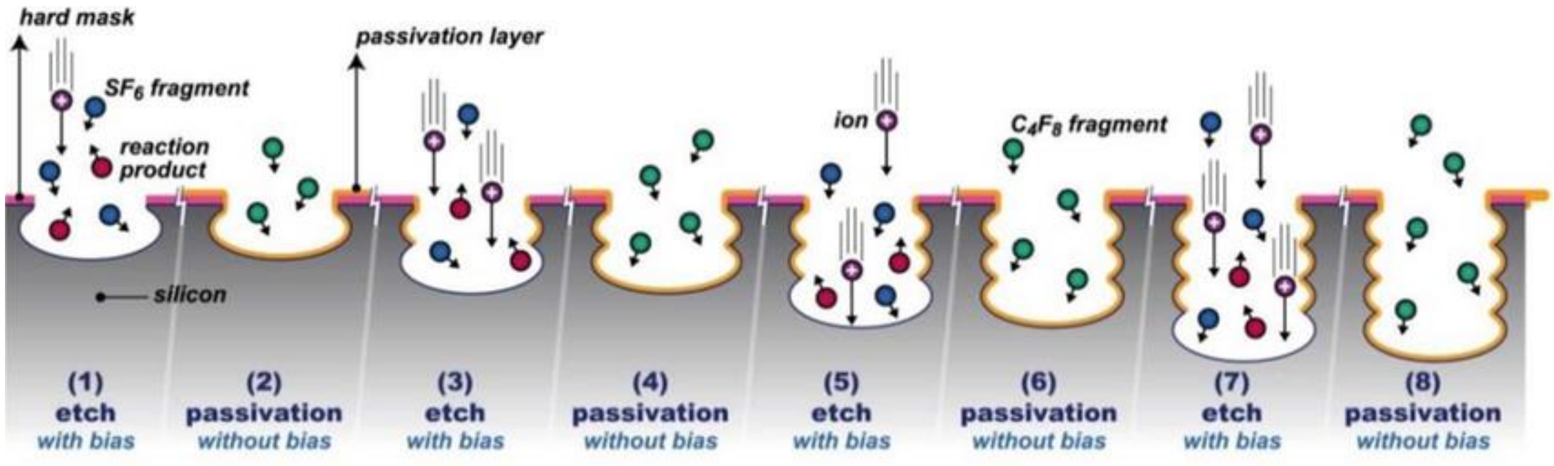
- ✓ The primary advantage of electron-beam lithography is that it can draw custom patterns (direct-write) with sub-10 nm resolution.



https://youtu.be/PWV9pvdRBNY

# Bosch process

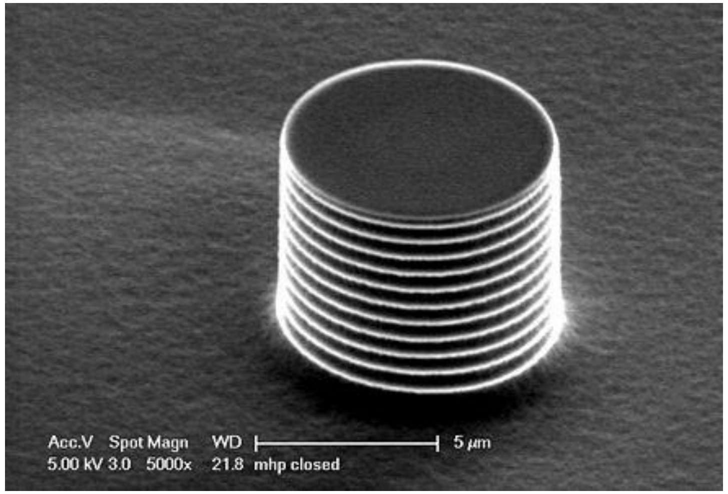
- ✓ The Bosch process alternates repeatedly between two modes to achieve nearly vertical structures.
- ✓ Nearly isotropic plasma etch $SF_6$ is often used for silicon
- ✓ Deposition of a chemically inert passivation layer

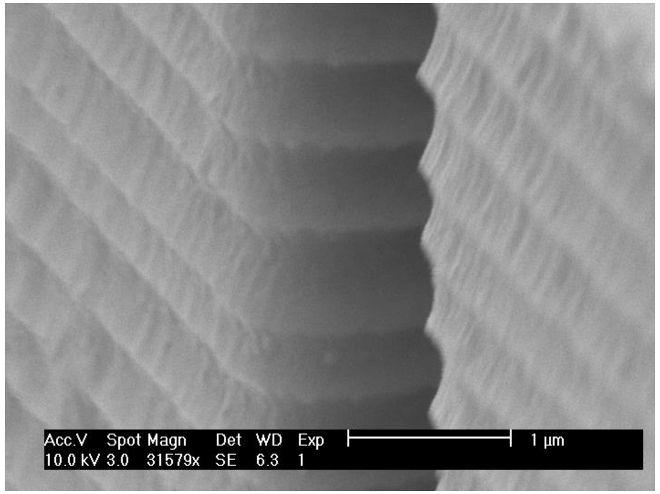


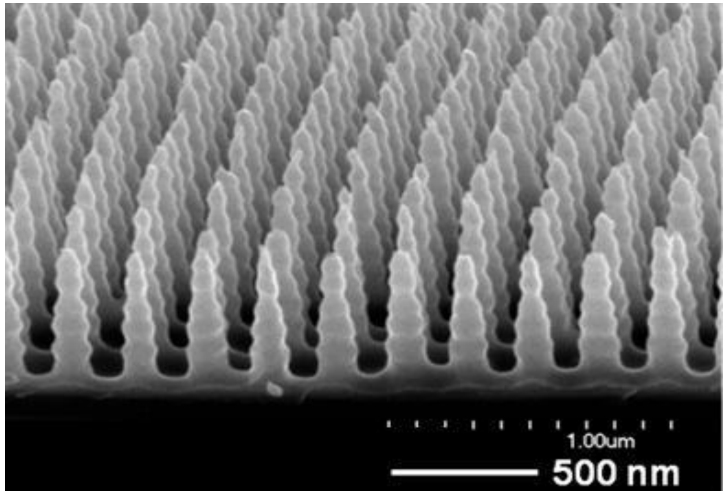
Conventional Bosch etch process scheme for etching silicon

# Bosch process

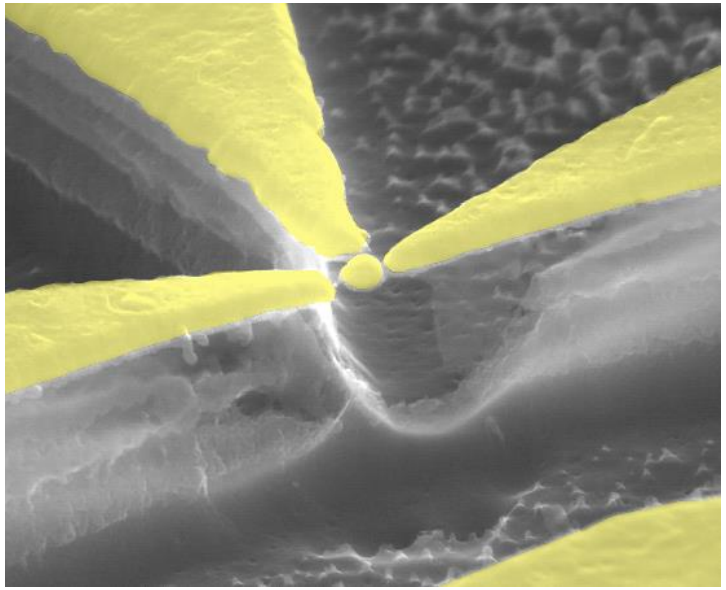
https://youtu.be/6Wva2a_4IA4

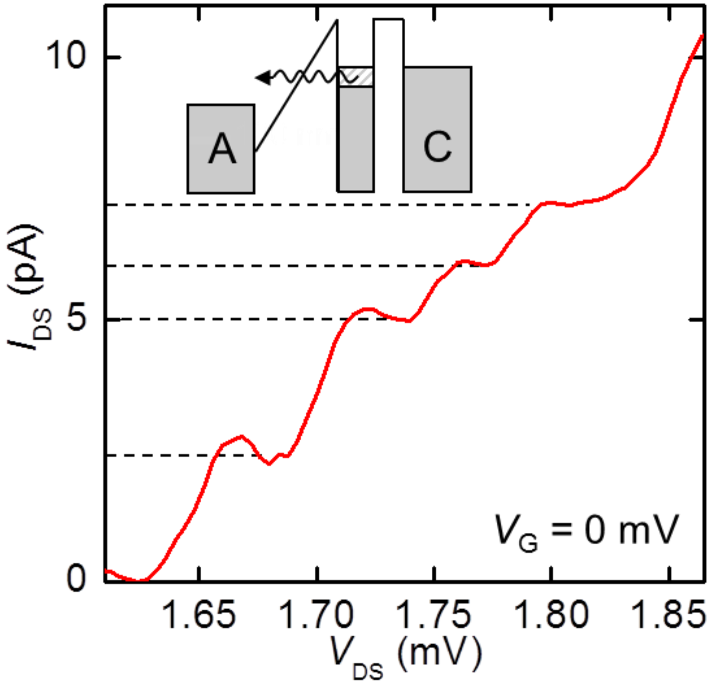






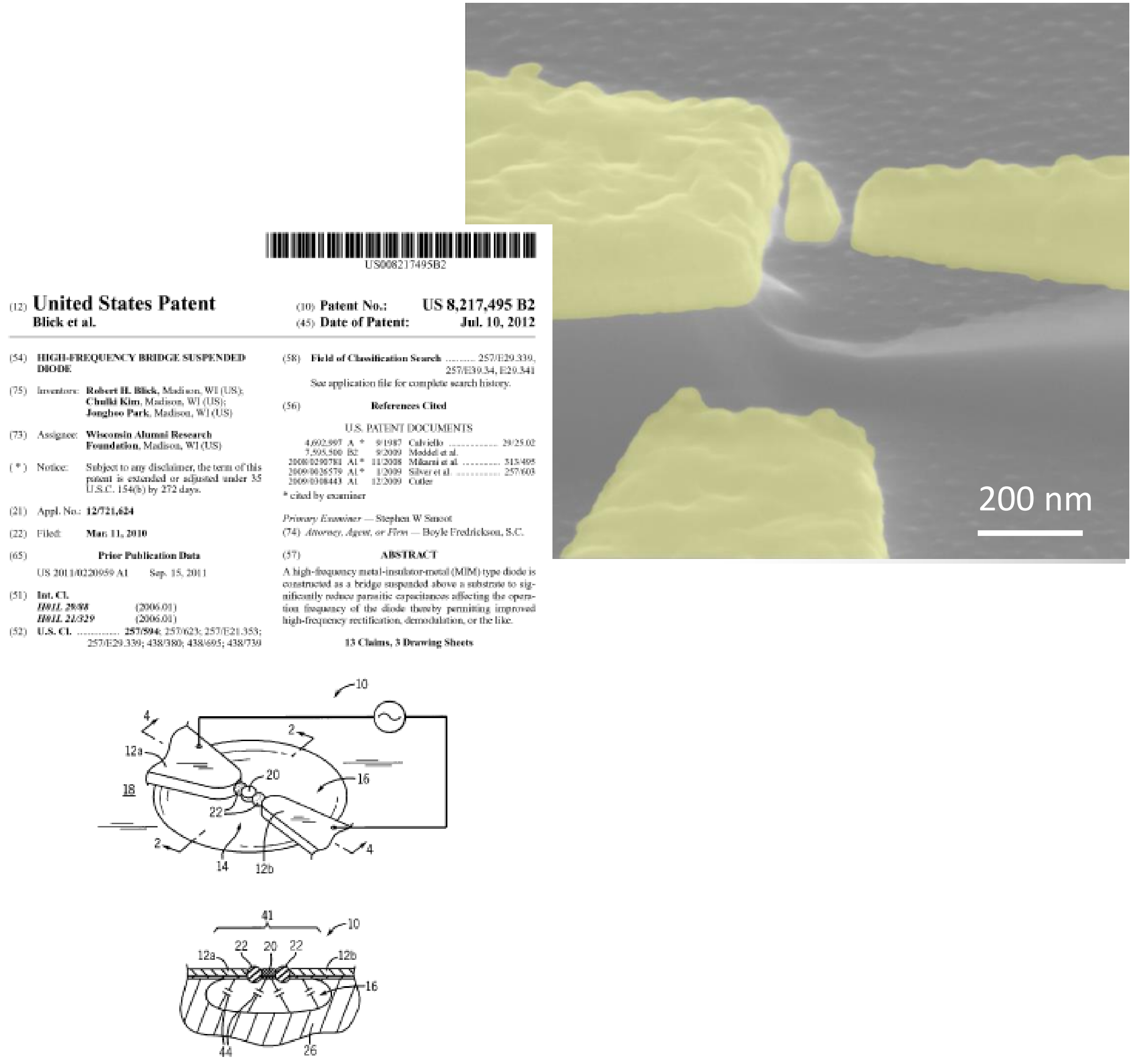
# Coulomb-controlled field electron emission in a suspended metallic island





C. Kim *et al.*, *Nano Lett.* 10, 615 (2010)

# Suspended metallic island



US008217495B2

(12) **United States Patent**
**Blick et al.**

(10) **Patent No.:** **US 8,217,495 B2**
(45) **Date of Patent:** **Jul. 10, 2012**

(54) **HIGH-FREQUENCY BRIDGE SUSPENDED DIODE**

(75) Inventors: **Robert H. Blick**, Madison, WI (US); **Chulki Kim**, Madison, WI (US); **Jonghoo Park**, Madison, WI (US)

(73) Assignee: **Wisconsin Alumni Research Foundation**, Madison, WI (US)

( * ) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 272 days.

(21) Appl. No.: **12/721,624**

(22) Filed: **Mar. 11, 2010**

(65) **Prior Publication Data**

US 2011/0220959 A1 Sep. 15, 2011

(51) **Int. Cl.**
*H01L 29/88* (2006.01)
*H01L 21/329* (2006.01)

(52) **U.S. Cl.** ............ **257/594**; 257/623; 257/E21.353; 257/E29.339; 438/380; 438/605; 438/739

(58) **Field of Classification Search** ......... 257/E29.339, 257/E39.34, E29.341
See application file for complete search history.

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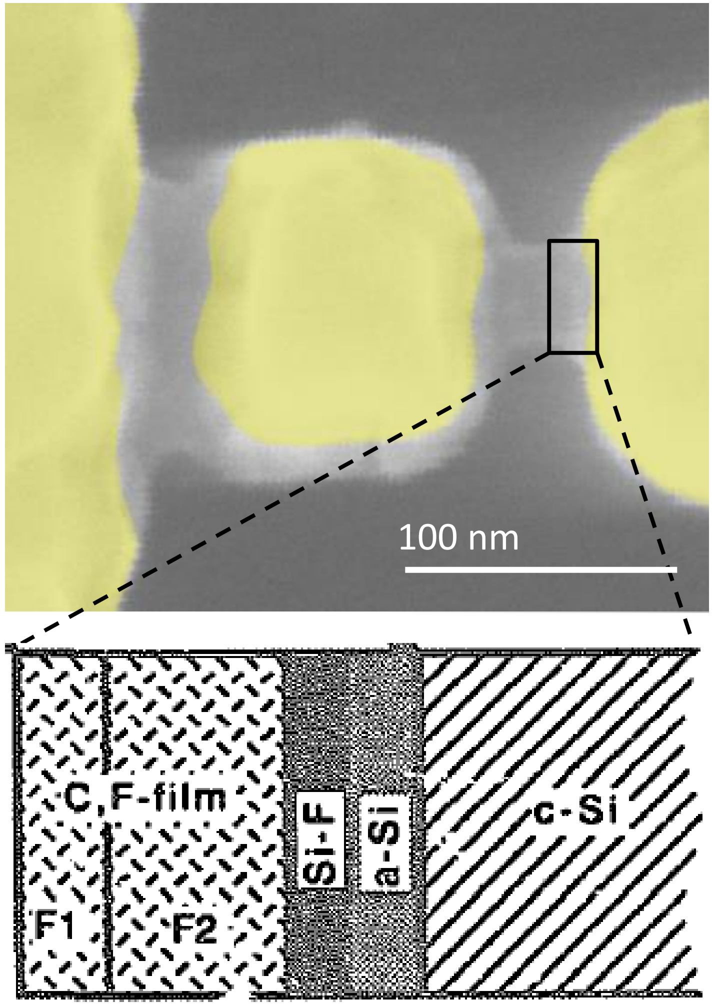
* cited by examiner

*Primary Examiner* — Stephen W Smoot
(74) *Attorney, Agent, or Firm* — Boyle Fredrickson, S.C.

(57) **ABSTRACT**

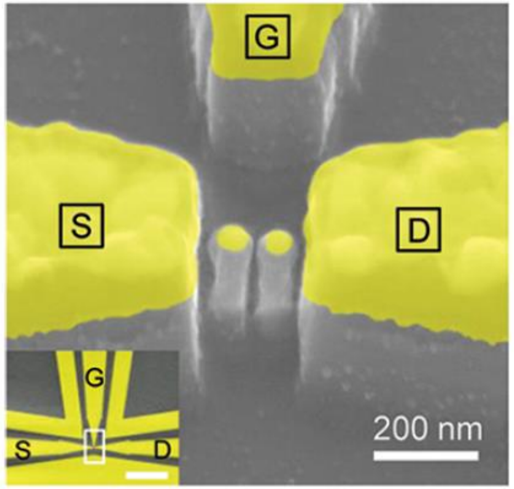
A high-frequency metal-insulator-metal (MIM) type diode is constructed as a bridge suspended above a substrate to significantly reduce parasitic capacitances affecting the operation frequency of the diode thereby permitting improved high-frequency rectification, demodulation, or the like.

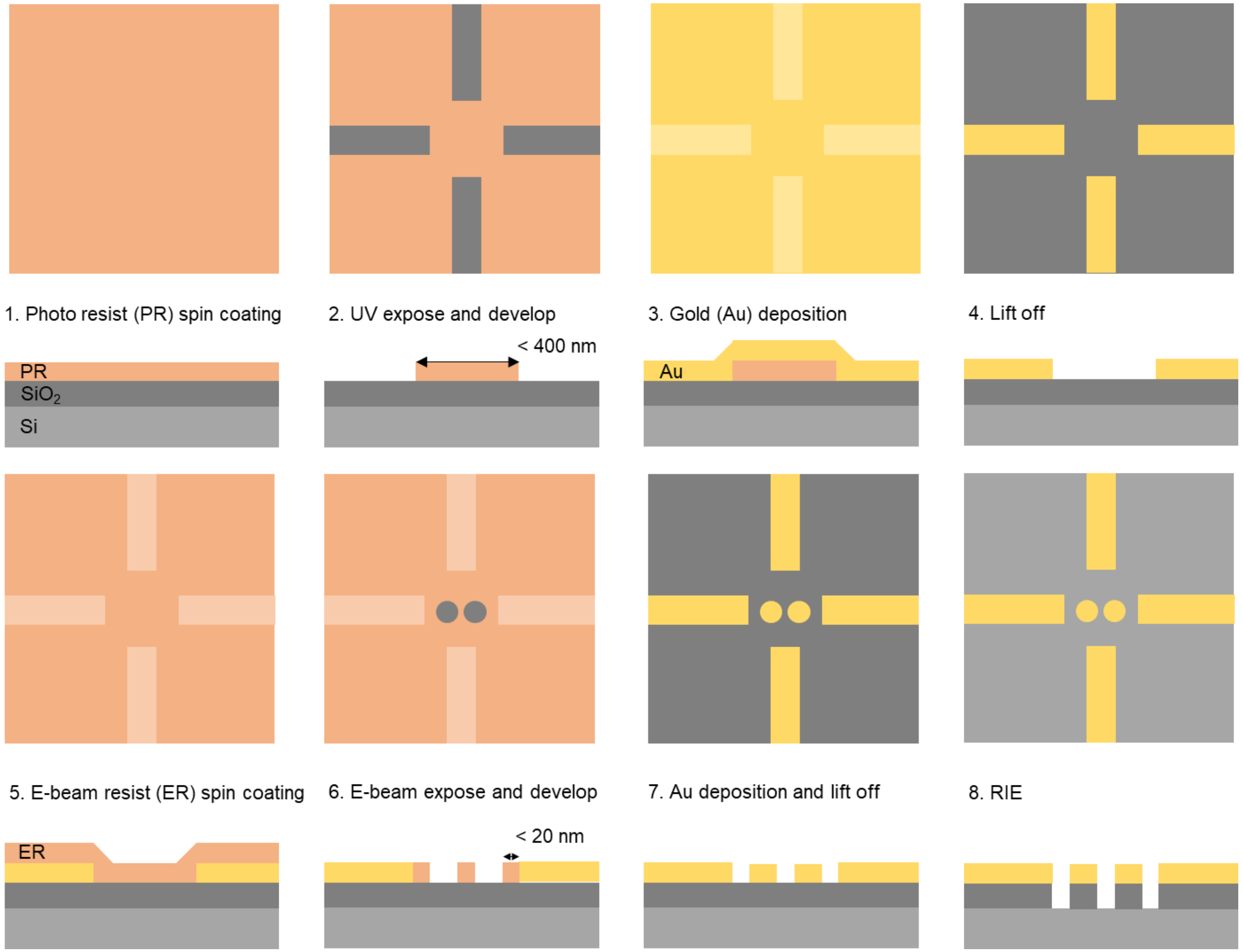
**13 Claims, 3 Drawing Sheets**



C. Kim *et al.*, *Phys. Status Solidi RRL* 4, 115 (2010)
C. Lejeune *et al., Revue Phys. Appl.* 24, 295 (1989)
Y. W. Zhu *et al.*, *Chem. Phys. Lett.* 419, 458 (2006)

# Coupled electron shuttles

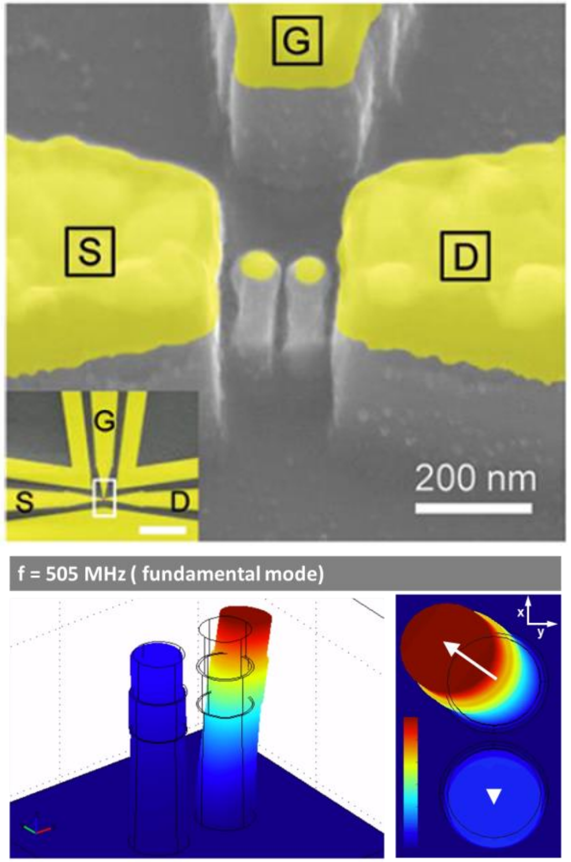


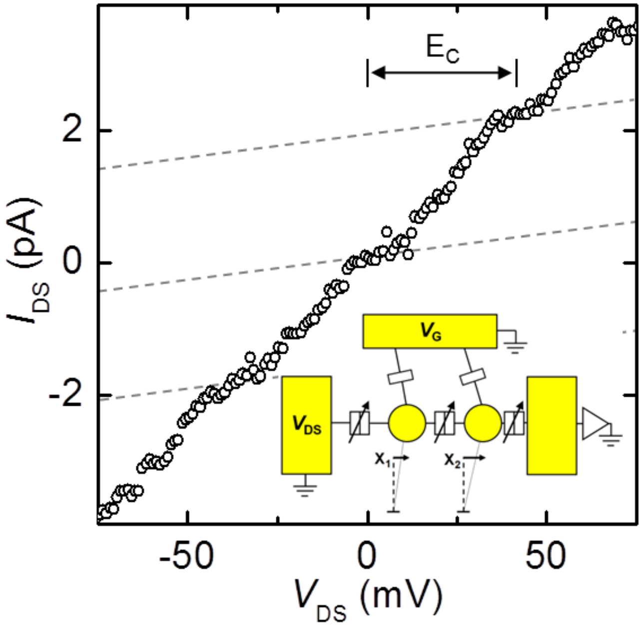


1. Photo resist (PR) spin coating
2. UV expose and develop
3. Gold (Au) deposition
4. Lift off
5. E-beam resist (ER) spin coating
6. E-beam expose and develop
7. Au deposition and lift off
8. RIE

C. Kim *et al.*, *Phys. Rev. Lett.* 105, 067204 (2010)

# I-V trace from coupled electron shuttles

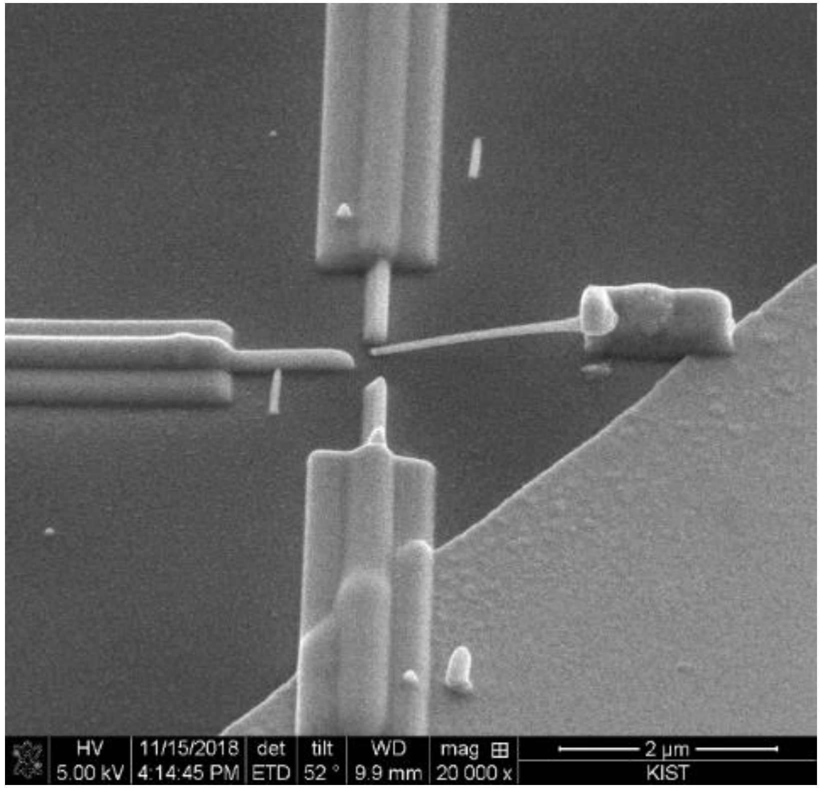


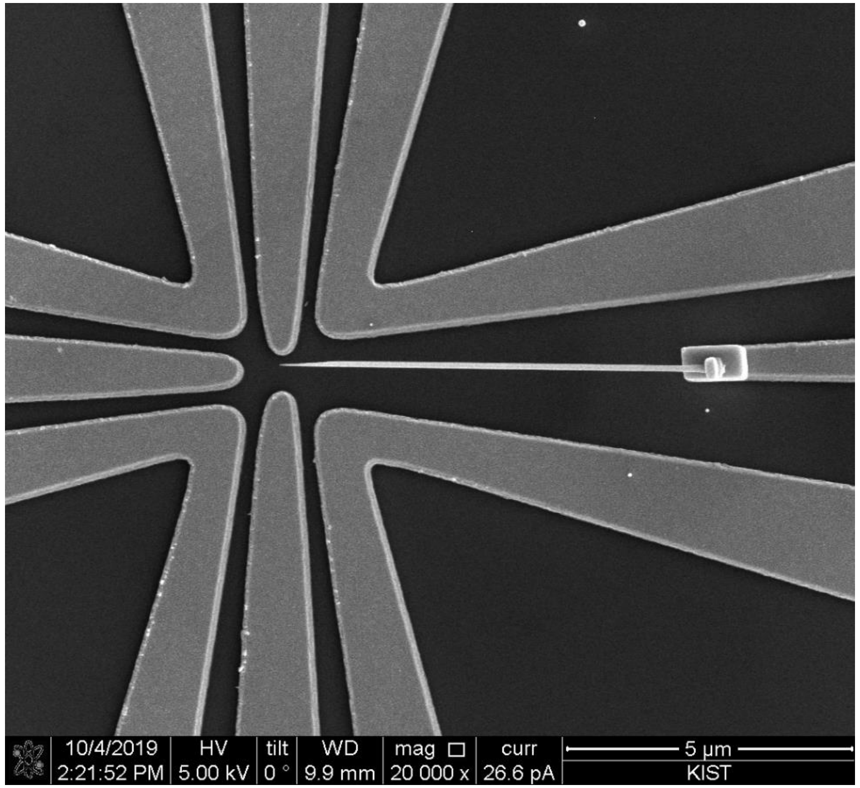


- Steplike current increase at room temperature
- Charging energy $E_C \sim 40$ meV
- Current modulation by gate voltages

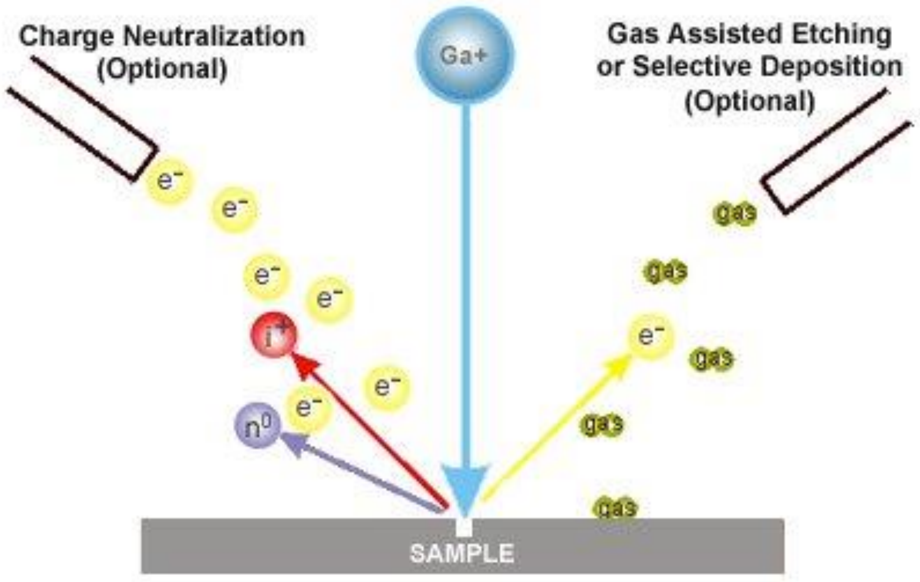
C. Kim *et al.*, *Phys. Rev. Lett.* 105, 067204 (2010)
C. Kim *et al.*, *ACS nano* 6, 651 (2012)

# Nanowire(NW)-based NEMS





# Focused Ion Beam (FIB)

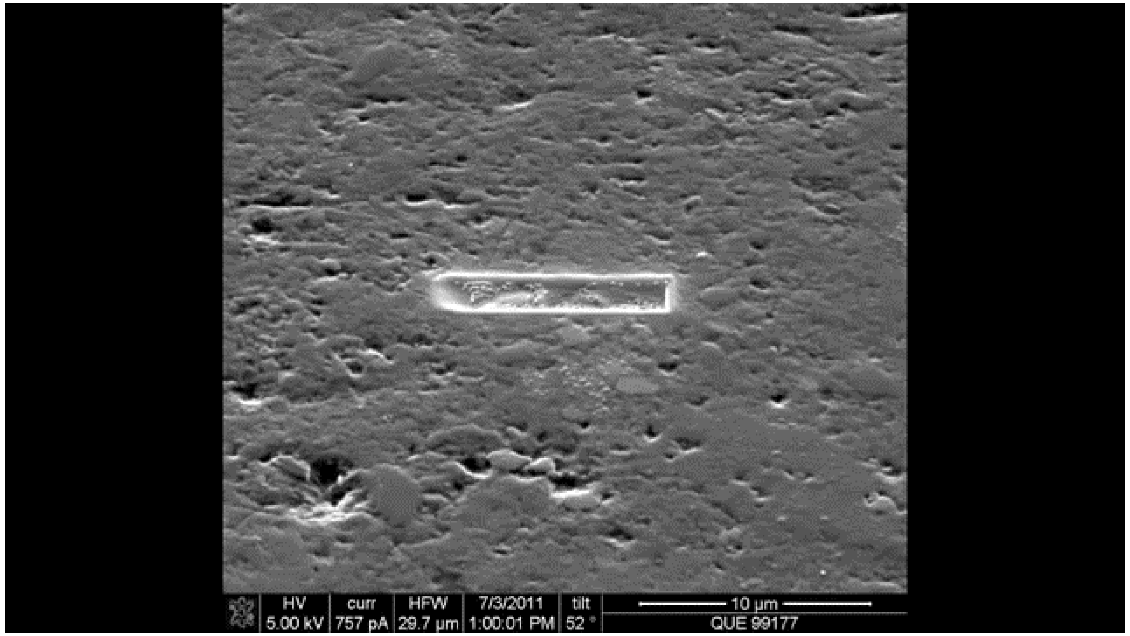


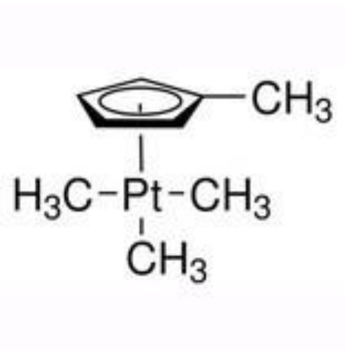
- Circuit modification
- Photomask repair
- TEM sample preparation of site specific locations

- ✓ FIB systems use a finely focused beam of ions (usually gallium) that can be operated at low beam currents for imaging or at high beam currents for site specific sputtering or milling.
- ✓ At higher primary currents, a great deal of material can be removed by sputtering, allowing precision milling of the specimen down to a sub micrometer or even a nanoscale.

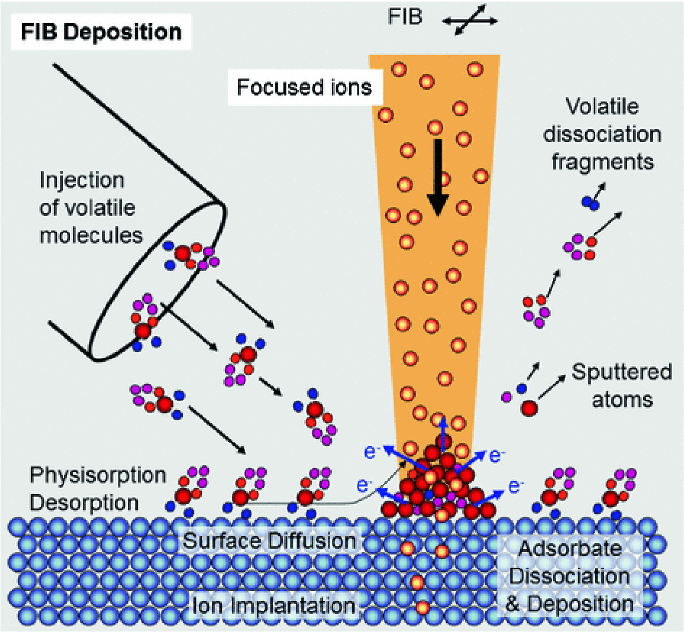
# Pt deposition using FIB

- ✓ FIB can also be used to deposit material via ion beam induced deposition. FIB-assisted chemical vapor deposition occurs when a gas is introduced to the vacuum chamber and allowed to chemisorb onto the sample.
- ✓ By scanning an area with the beam, the precursor gas will be decomposed into volatile and non-volatile components. The non-volatile component remains on the surface as a deposition.





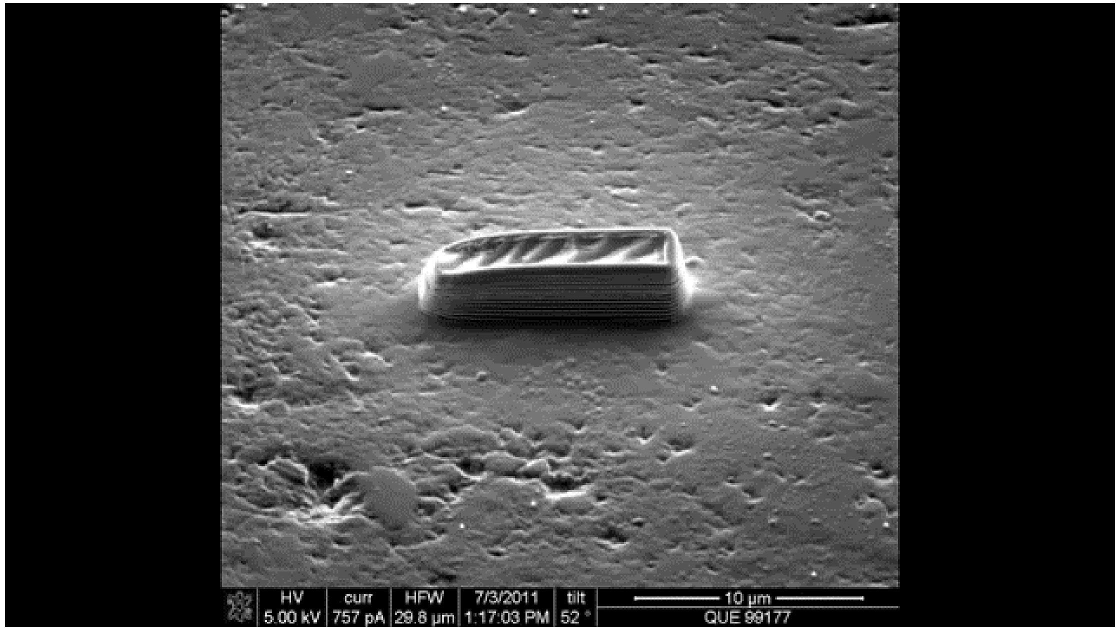
(Pt, Co, C, Au)



https://youtu.be/vNOpzDViAhE

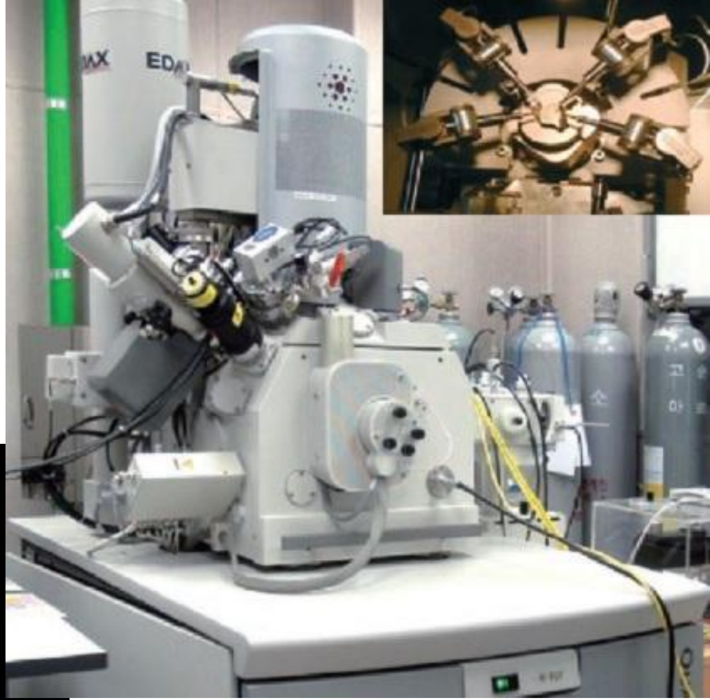
# FIB Etching

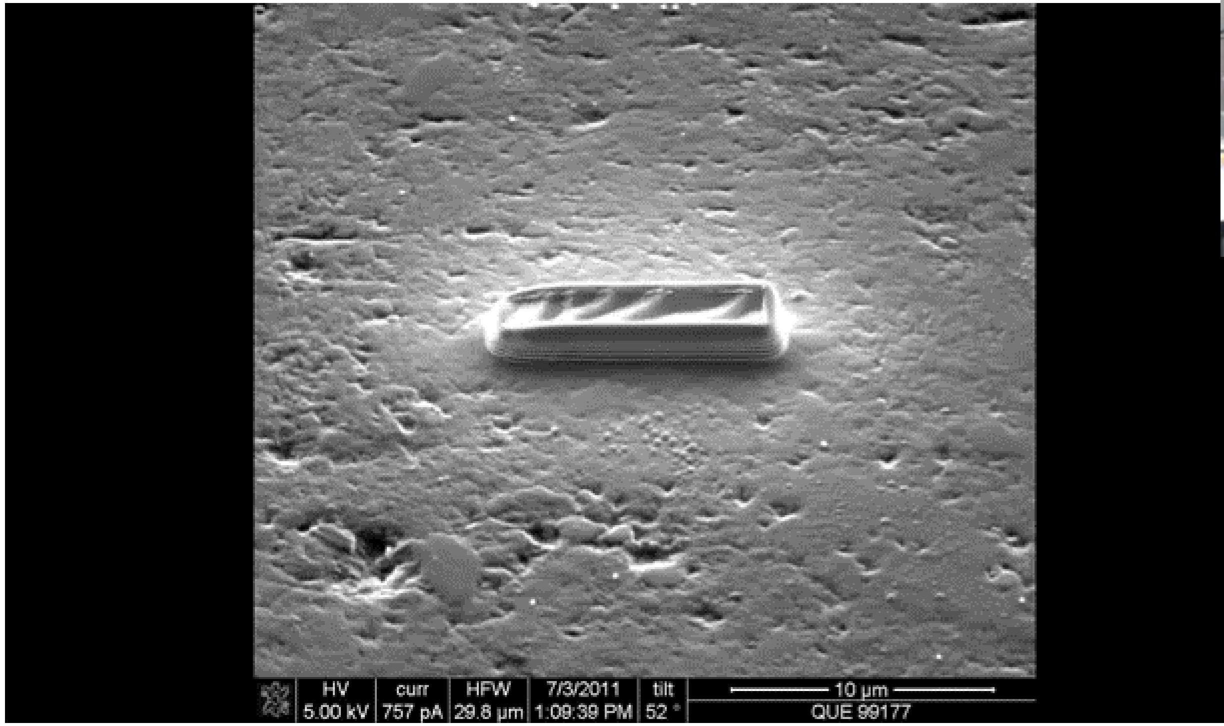
- ✓ FIB is inherently destructive to the specimen. When the high-energy gallium ions strike the sample, they will sputter atoms from the surface.
- ✓ Gallium atoms will also be implanted into the top few nanometers of the surface, and the surface will be made amorphous.
- ✓ Because of the sputtering capability, the FIB is used as a micro- and nano-machining tool, to modify or machine materials at the micro- and nanoscale.



https://youtu.be/vNOpzDViAhE

# Lifting out using FIB





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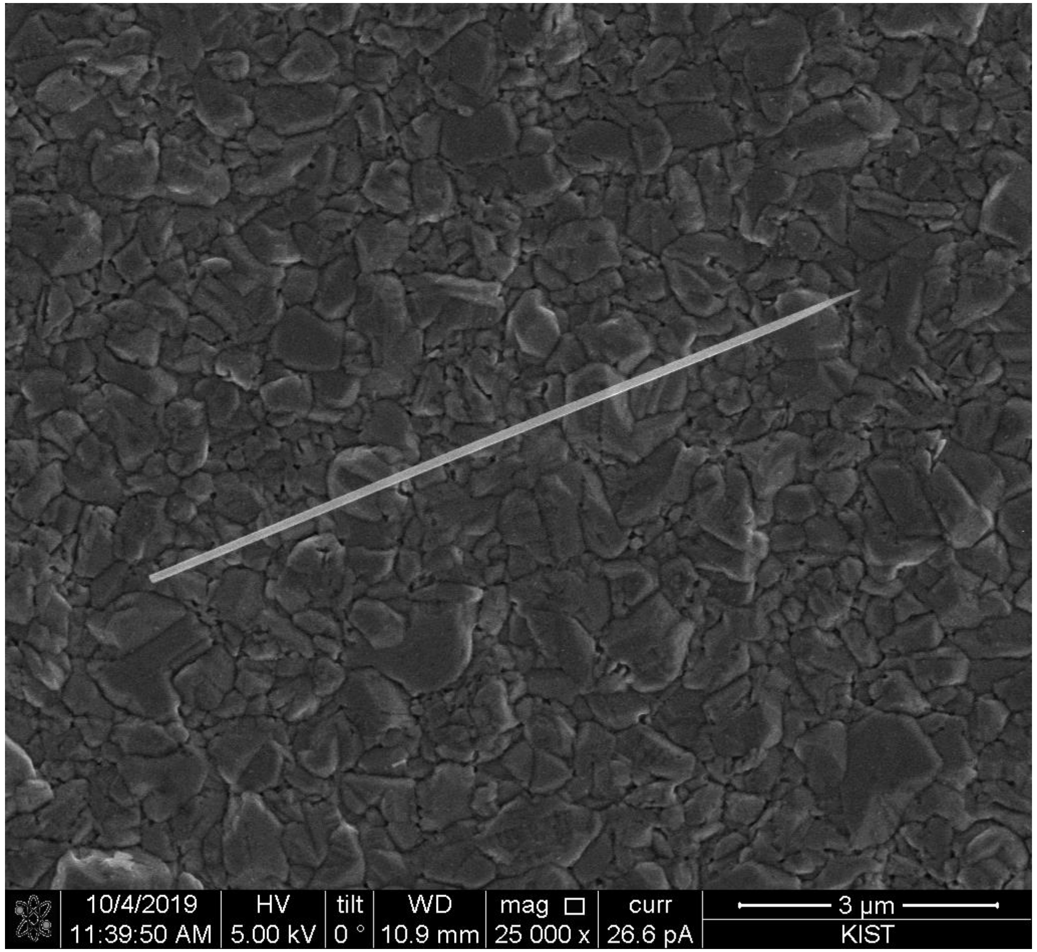
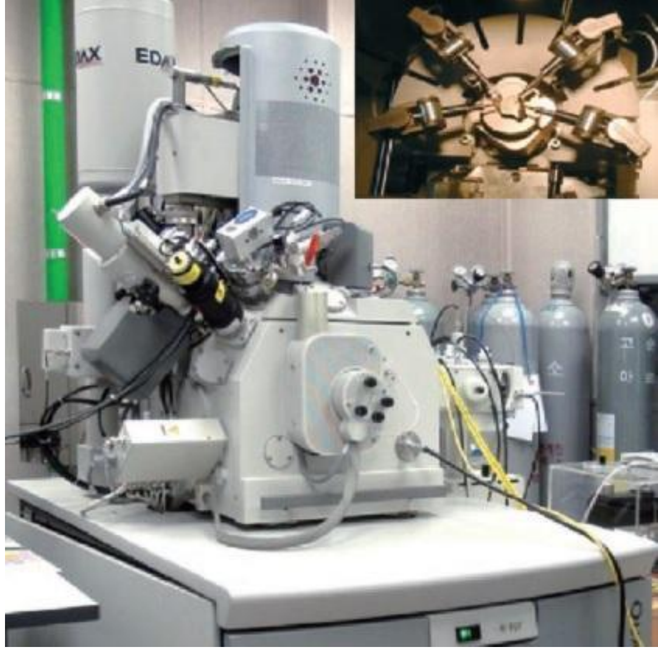
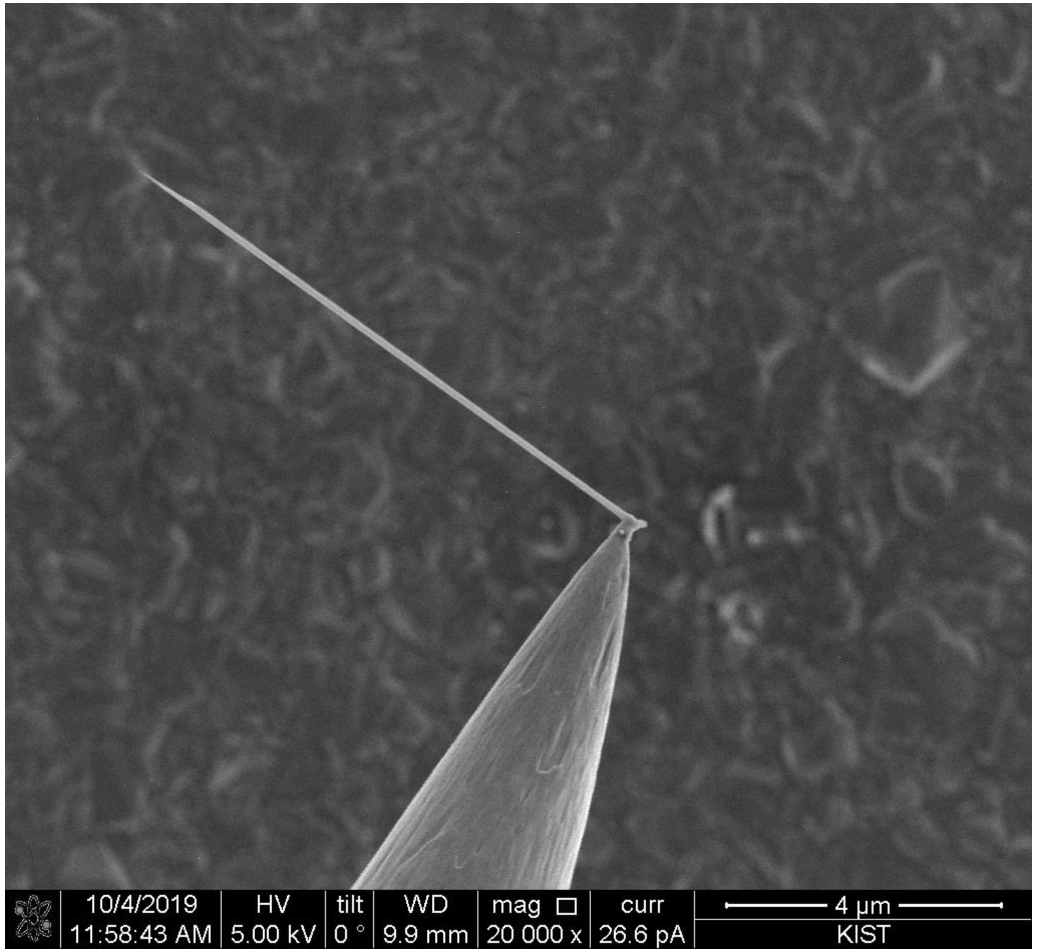
# NW-based NEMS Fabrication



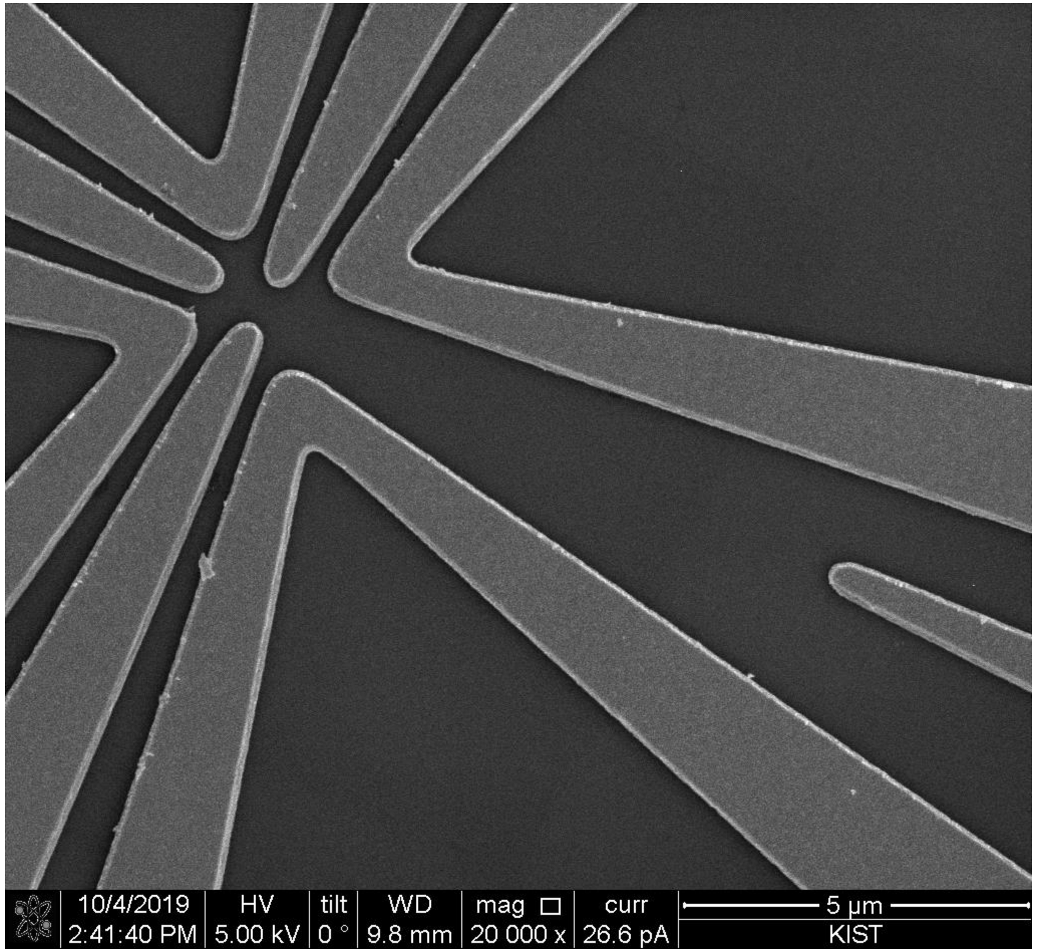
InGaAs nanowire

# NW-based NEMS Fabrication

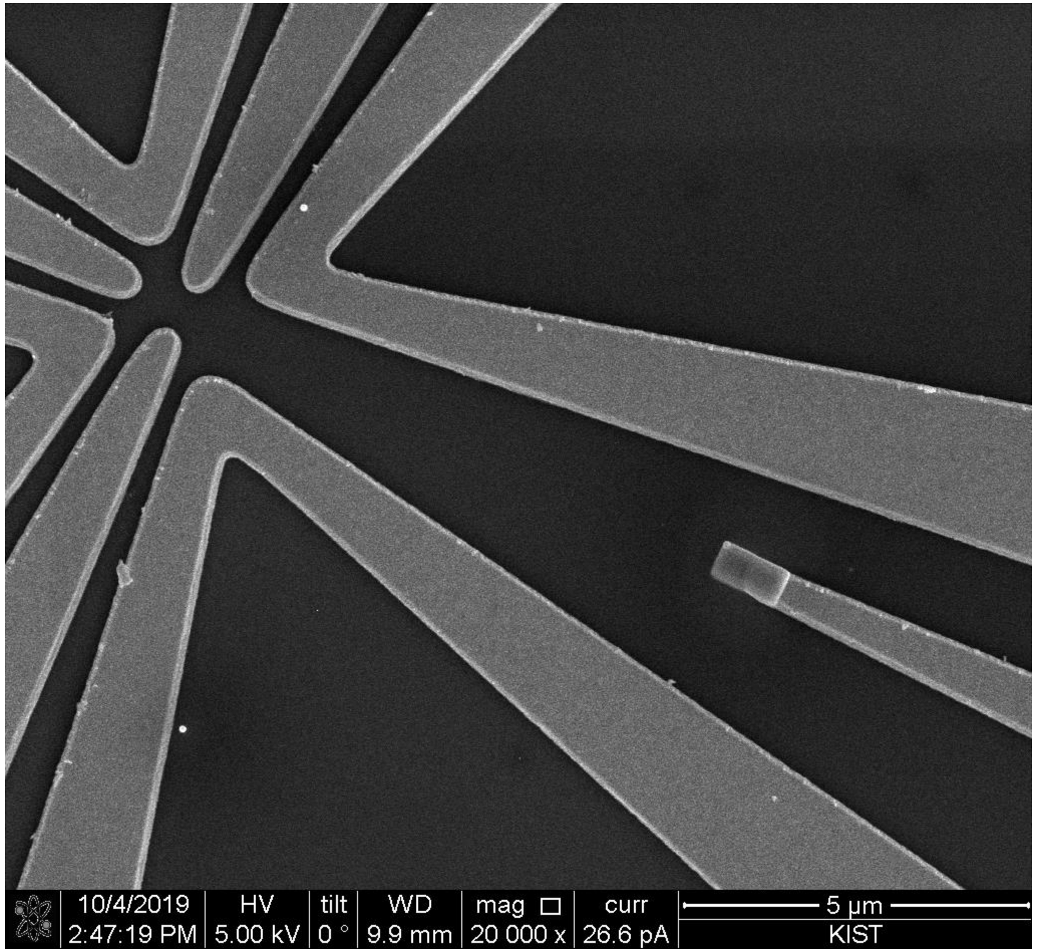




# NW-based NEMS Fabrication



# NW-based NEMS Fabrication



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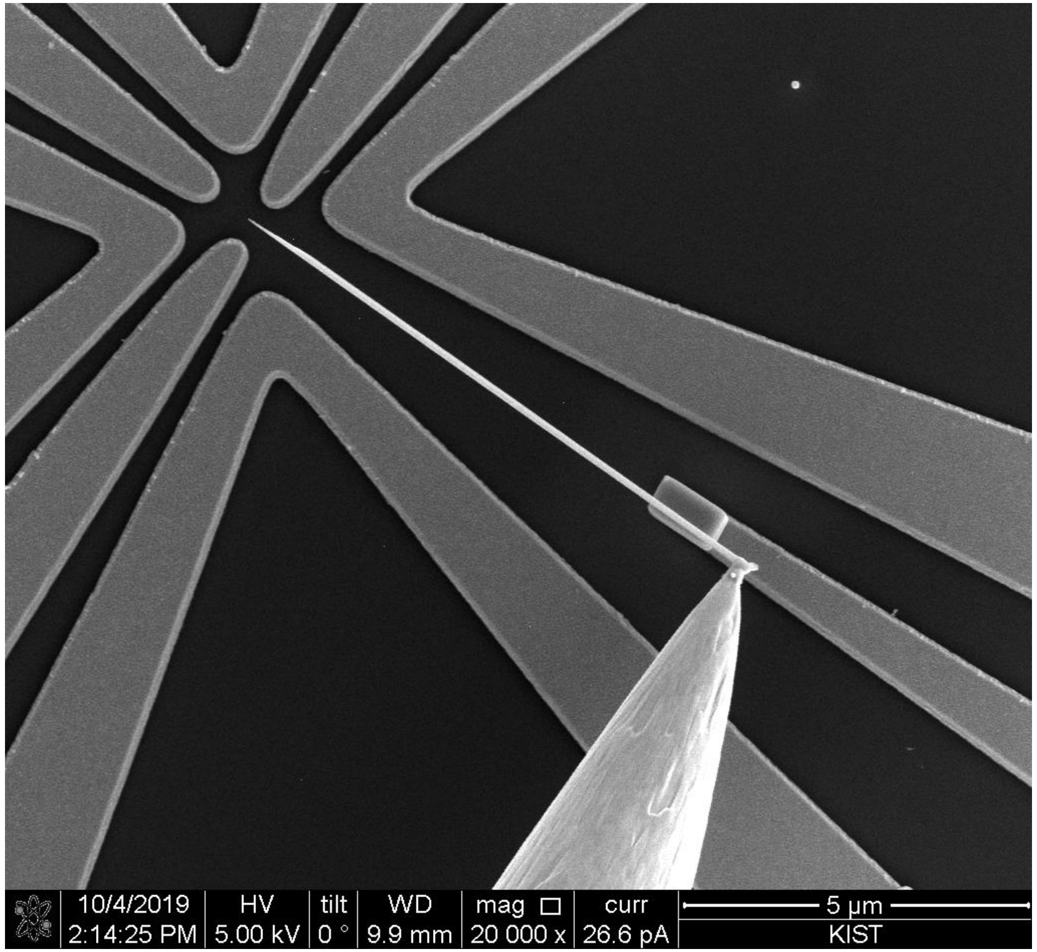

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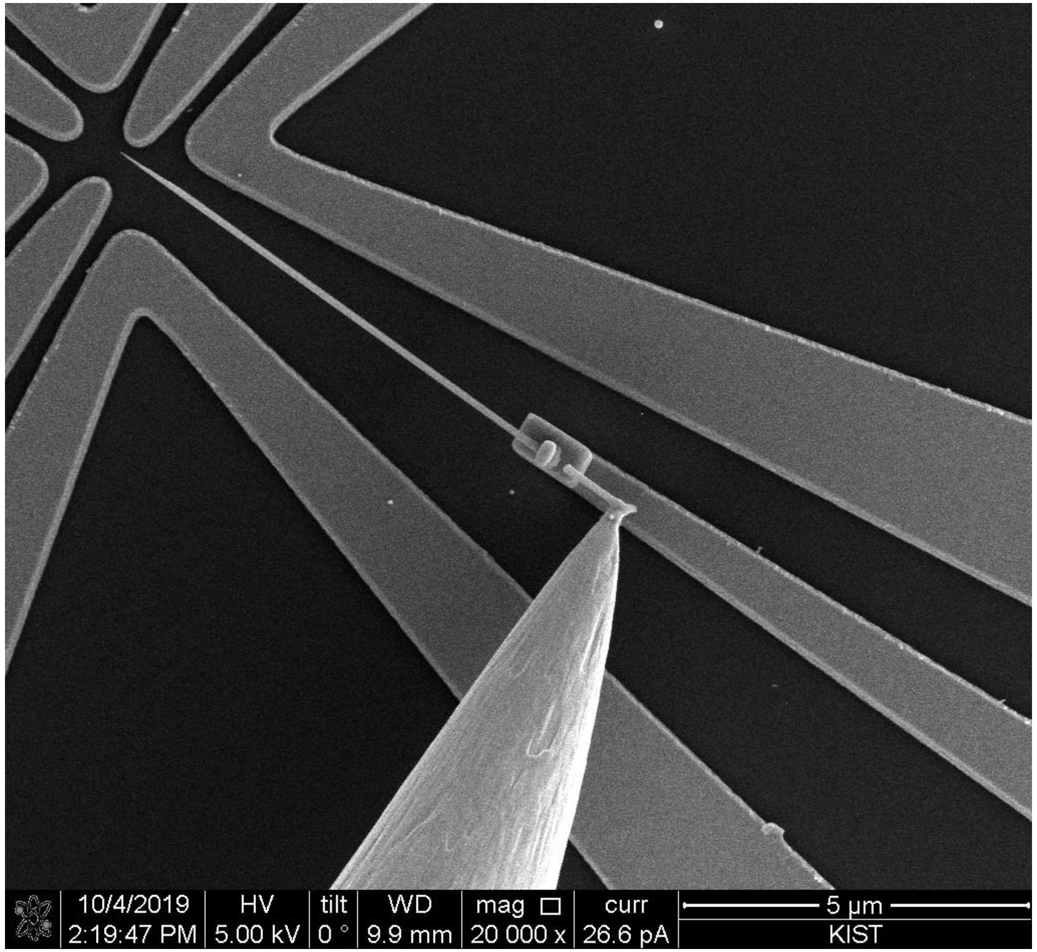
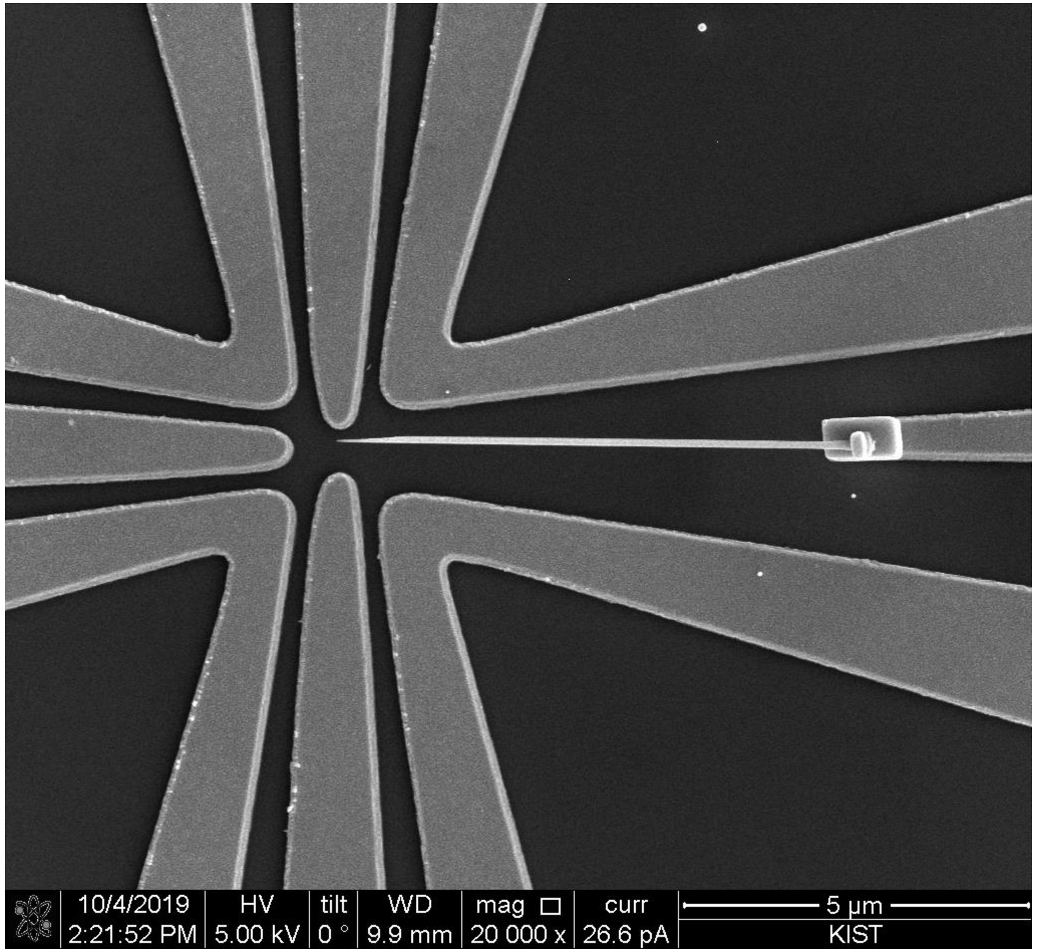
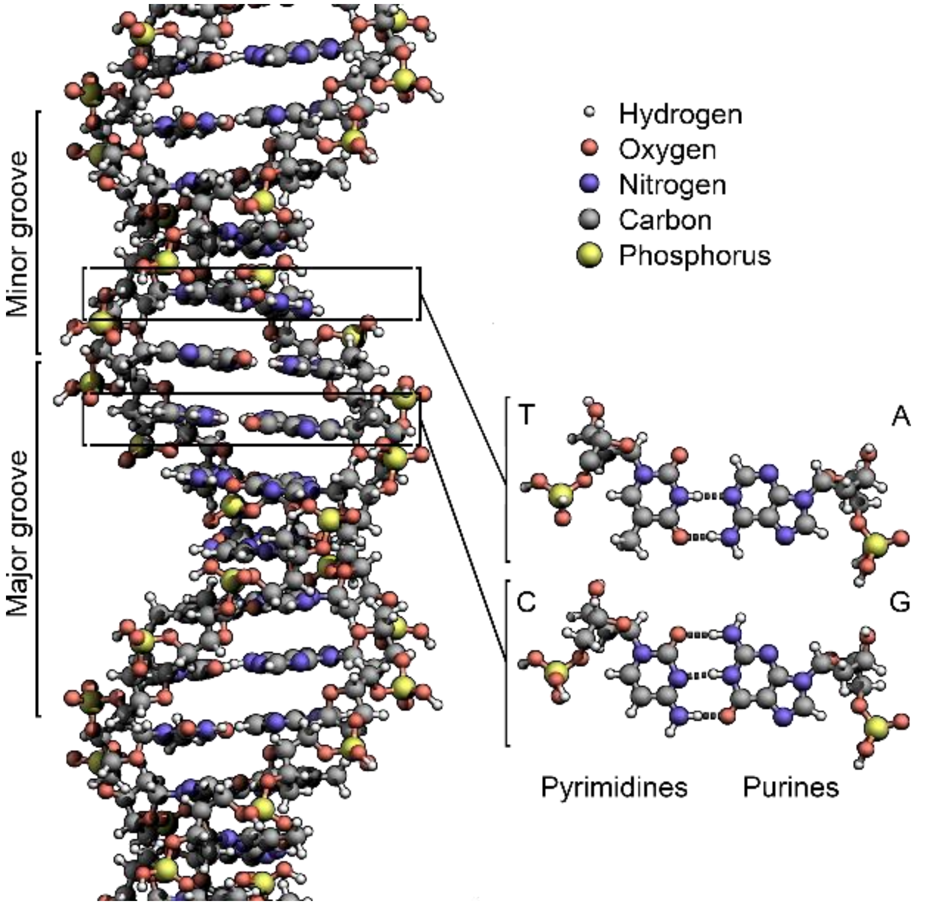


# NW-based NEMS Fabrication



# DNA as materials

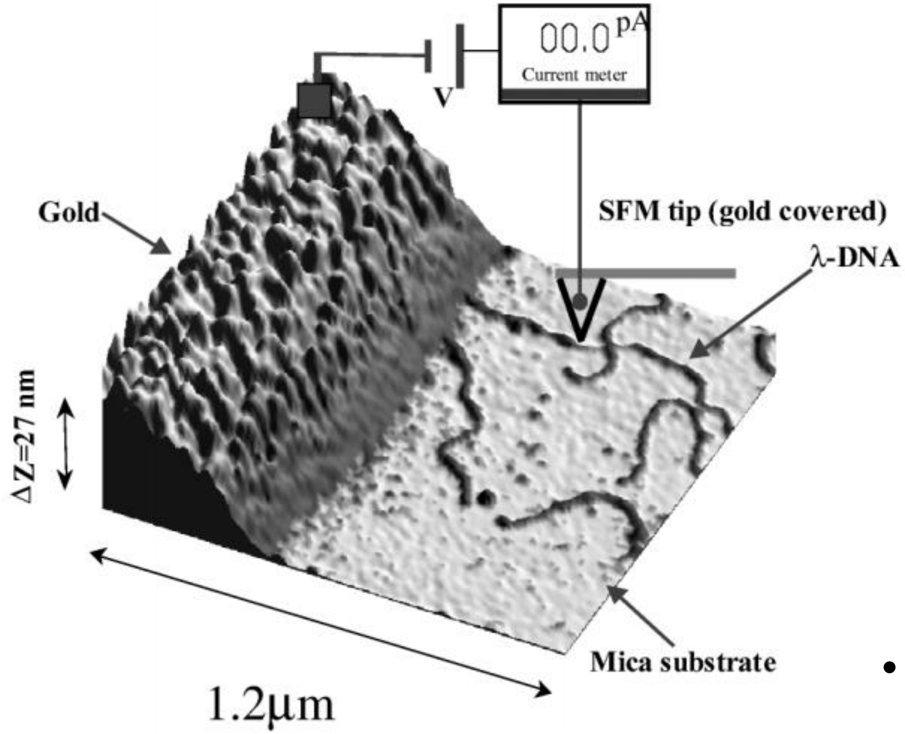
- ✓ Chemically stable : hereditary material in humans and almost all other organisms
- ✓ Sub-nanoscale engineering : a code made up of adenine(A), cytosine(C), guanine(G), and thymine (T)
- ✓ Self-assembly : enable to make nano-structure intentionally
- ✓ Abundant : cost-effective



R. G. Endres *et al.*, Rev. Mod. Phys. 76, 195 (2004)

# Studies on electrical properties of DNA

**Class 1**: DNA is an insulator at room temperature, as found by Braun et al. (1998), de Pablo et al. (2000), Strom et al. (2001), and Zhang et al. (2002).



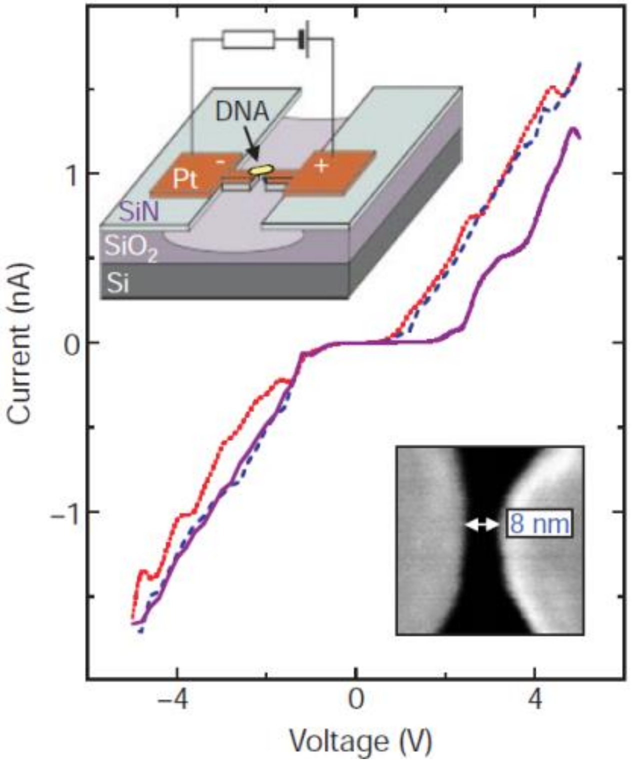
- The lower limit for the resistivity ~ $10^6$ Ω cm

P. J. de Pablo *et al.*, *Phys. Rev. Lett.* 85, 4992 (2000)

# Studies on electrical properties of DNA

**Class 1**: DNA is an insulator at room temperature, as found by Braun et al. (1998), de Pablo et al. (2000), Strom et al. (2001), and Zhang et al. (2002).

**Class 2**: DNA is a true wide-bandgap semiconductor at all temperature, as measured by Porath et al. (2000) and by Rakitin et al. (2001).



- Poly(G)-poly(C) DNA molecules (30 bp)
- ~ 8 nm separation
- without any functional group at the termini of the double helix

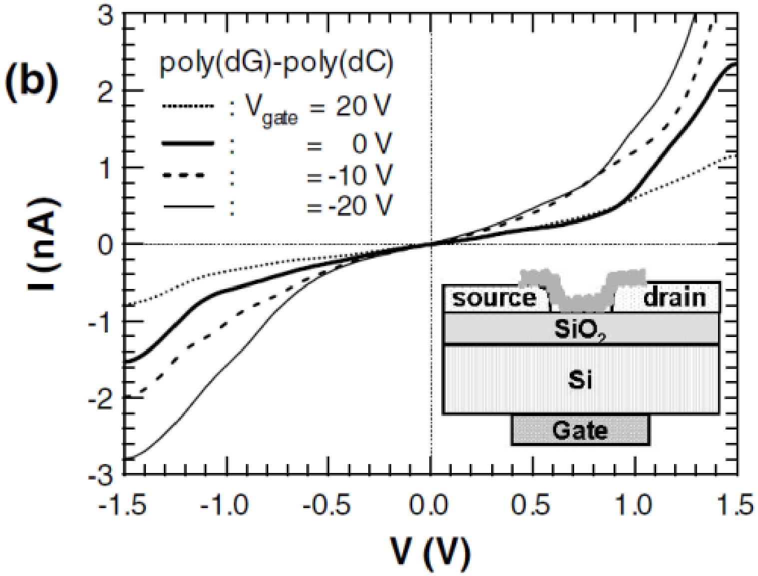
D. Porath *et al*., *Nature* 403, 635 (2000)

# Studies on electrical properties of DNA

**Class 1**: DNA is an insulator at room temperature, as found by Braun et al. (1998), de Pablo et al. (2000), Strom et al. (2001), and Zhang et al. (2002).

**Class 2**: DNA is a true wide-bandgap semiconductor at all temperature, as measured by Porath et al. (2000) and by Rakitin et al. (2001).

**Class 3**: DNA is Ohmic or nearly Ohmic at room temperature and is insulating at low temperatures, as found by Fink and Schonenberger, Cai et al. (2000), Tran et al. (2000), Rakitin et al. (2001), Yoo et al. (2001), and Hartzell et al. (2003).



K. –H. Yoo *et al.*, *Phys. Rev. Lett.* 87, 635 (2001)

# Studies on electrical properties of DNA

**Class 1**: DNA is an insulator at room temperature, as found by Braun et al. (1998), de Pablo et al. (2000), Strom et al. (2001), and Zhang et al. (2002).

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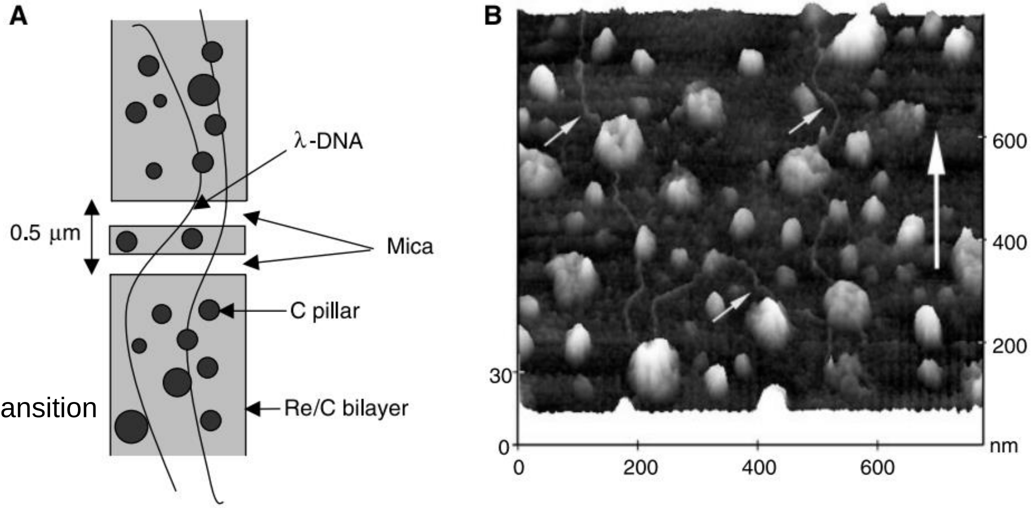
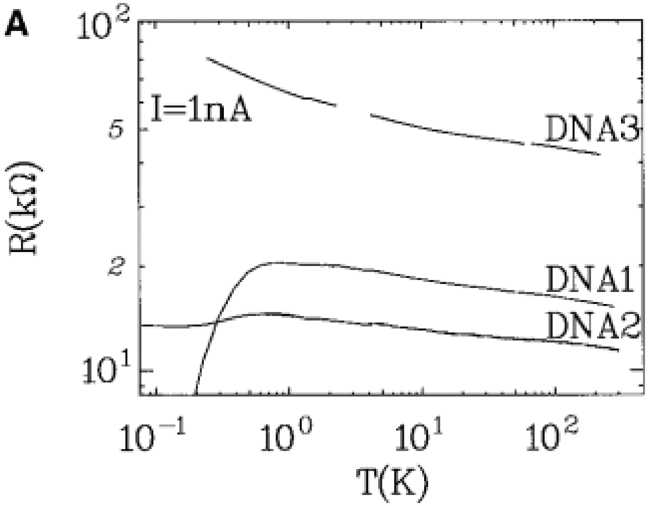
**Class 4**: DNA is truly metallic down to low temperature, as suggested by Kasumov et al. (2001). - superconductivity



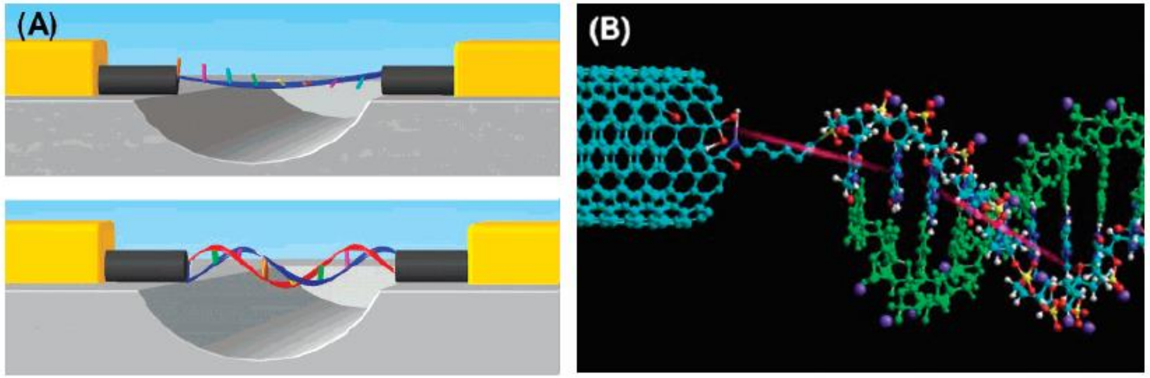
Rhenium/carbon electrodes

Superconduction transition around 1K



A. Y. Kasumov *et al.*, *Science* 291, 280 (2001)

# Direct electrical measurements on single-molecule genomic DNA using single-walled carbon nanotubes

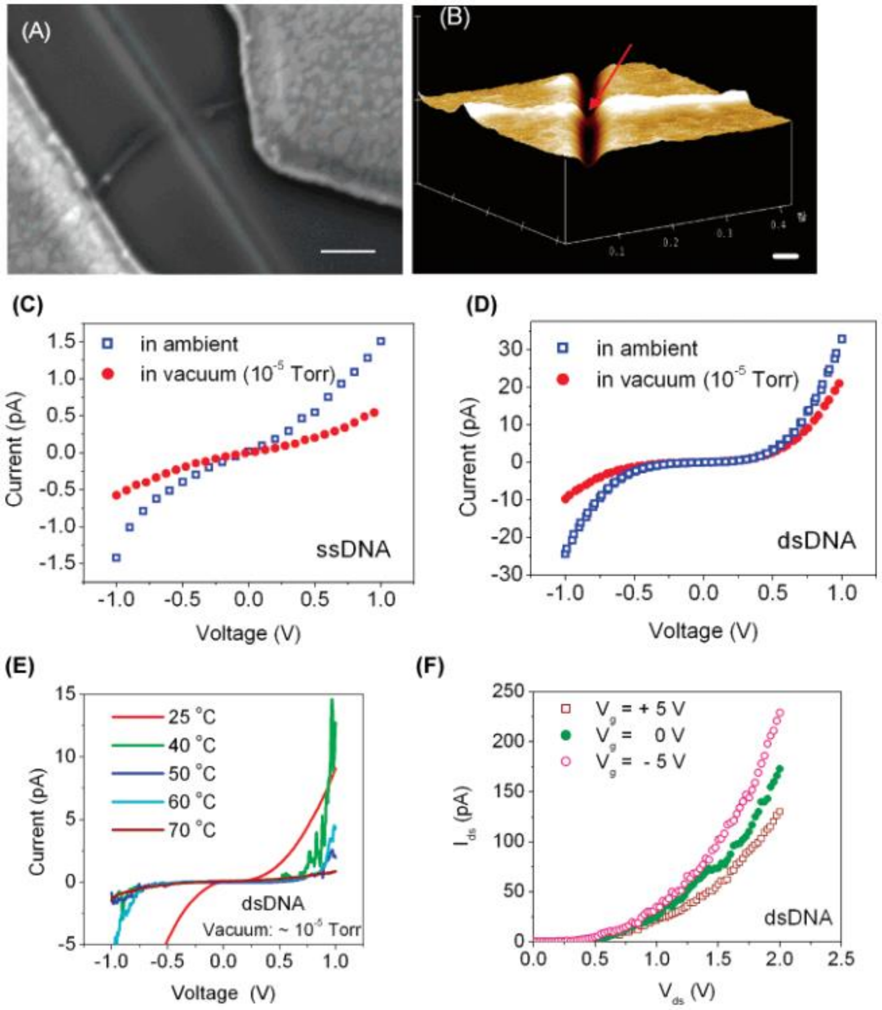


S. Roy et al., Nano Lett. 8, 26 (2008).

- A novel platform based on SWNT nanoelectrodes for directly probing the dc conductivity in DNA.

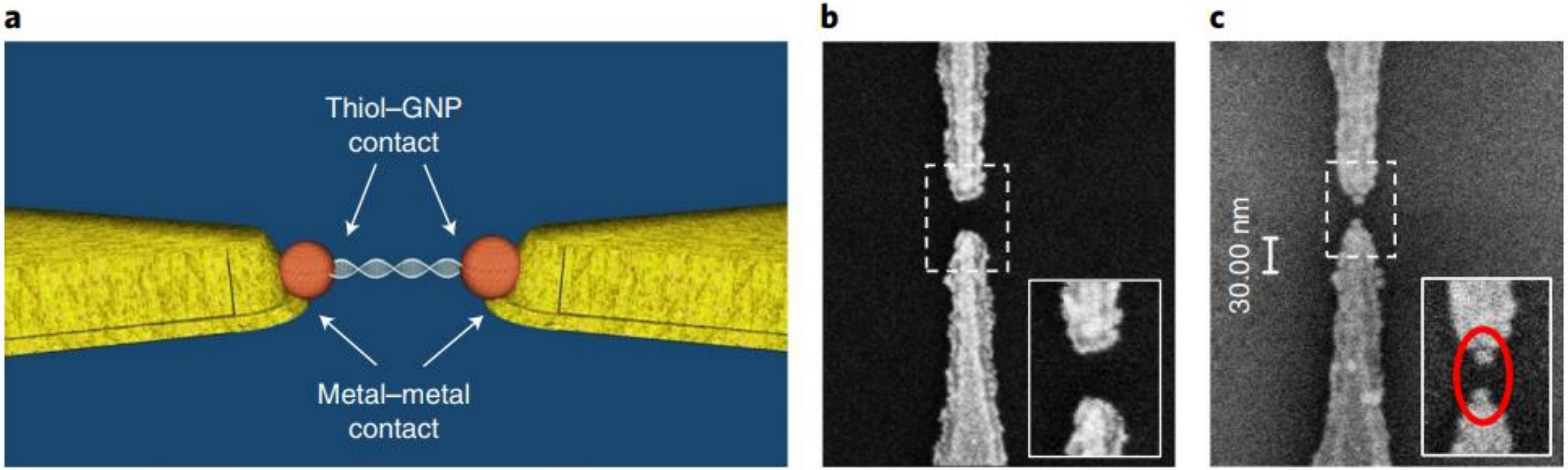
  - 80 base pairs (~27nm) of single- and double stranded DNA
  - Covalent bonding between an amine-terminated ssDNA and a carboxyl-functionalized SWNT

- Application of the back-gate voltage revealed that the bridging DNA molecule forms a p-type semiconducting channel between the SWNT electrodes



S. Roy *et al.*, *Nano Lett. 8*, 26 (2008).

# Backbone charge transport in double-stranded DNA

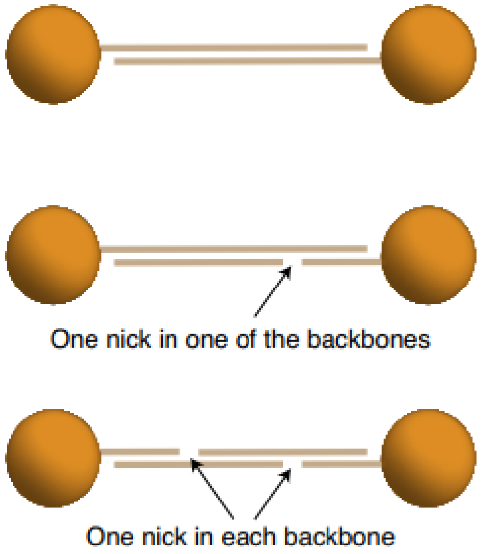


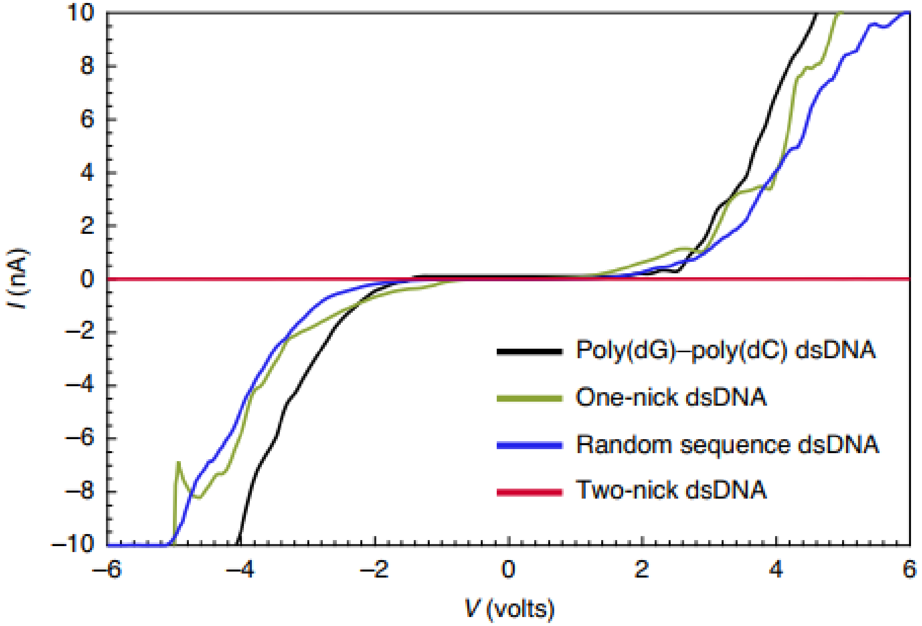
- Electrical measurements through individual conjugates of 30 nm long dsDNA molecules with two gold nanoparticles (dimer)
  : the 3’ end of each of the DNA strands is bonded to one of the GNPs through a $C_3$ thiol linker.

- Dielectrophoresis trapping of the dimer

R. Zhuravel *et al.*, *Nat. Nanotech. doi.org/10.1038/s41565-020-0741-2* (2020)

# Backbone charge transport in double-stranded DNA





- I-V curves of the different types of dimers at 5K.
- One nick in one of the backbones has no impact on the current, whereas two nicks suppress the current below the noise floor.

R. Zhuravel *et al., Nat. Nanotech. doi.org/10.1038/s41565-020-0741-2* (2020)

# Safety

- ✓ Follow the guideline (Acid, Gas, etc.)
- ✓ Apply safety tools (guard, gloves, safety glass etc.)
- ✓ Remember buddy system

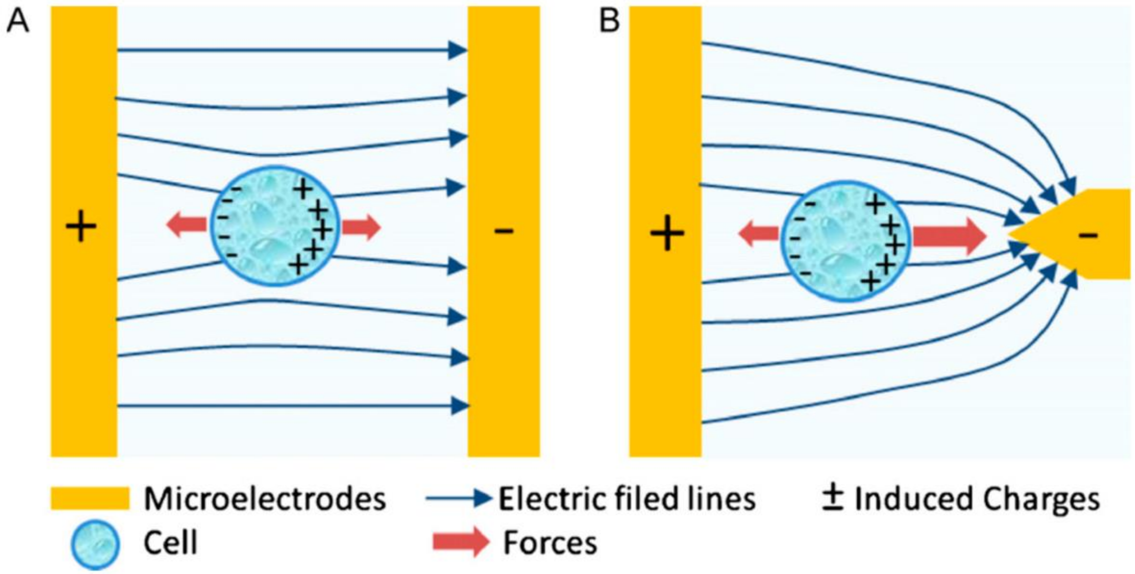
# Summary

- Discussed top-down and bottom-up approach
- Inctroduced fabrication processes for field effect transistor (FET) with dual gates
- Introduced fabrication processes for electron shuttles as Nanoelectromechanical systems (NEMS)
- Briefly discussed the possibility of DNA as a material for self-assembled nanostructure

# Thanks

# Dielectrophoresis (DEP)

- ✓ Motion of a particle is produced by the interaction of a non-uniform electric field with the induced effective dipole moment of the particle. A force is exerted on a dielectric particle when it is subjected to a non-uniform electric field.
- ✓ The strength of the force depends strongly on the medium and particles electrical properties, on the particles shape and size, as well as on the frequency of the electric field.



Clausius-Mossotti factor

Time-averaged DEP force

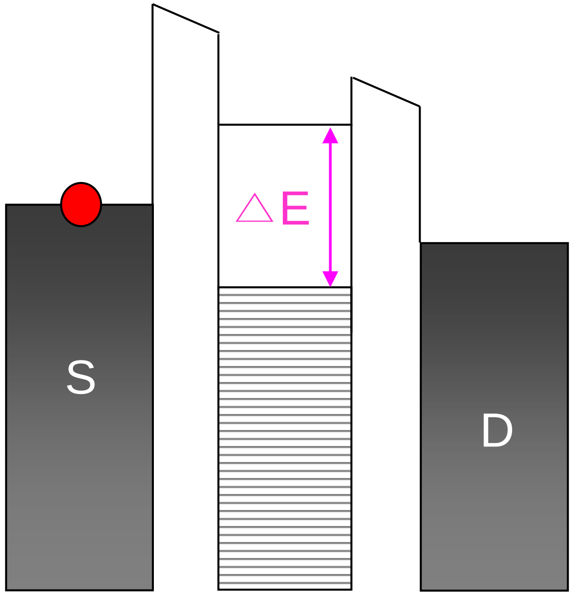
$$\langle F_{DEP} \rangle = 2\pi\epsilon_m a^3 Re[f_{CM}]\nabla|E|^2$$

Positive DEP : Real ($f_{CM}$) > 0
Particles attracted towards high fields

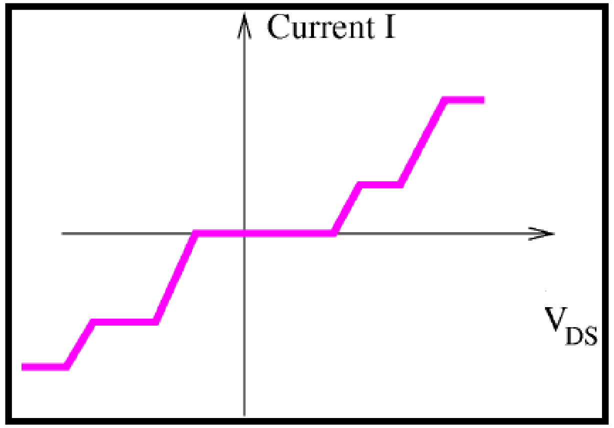
Negative DEP : Real ($f_{CM}$) < 0
Particles repelled from high fields

# Coulomb Blockade

$$\Delta E = \frac{e^2}{C_{eq}}$$



Source-drain bias voltage control



Gate voltage control